# LOW COST HIGH EFFICIENCY SCREEN PRINTED SOLAR CELLS ON CZ AND EPITAXIAL SILICON

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# LOW COST HIGH EFFICIENCY SCREEN PRINTED SOLAR CELLS ON CZ AND EPITAXIAL SILICON

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*This thesis work is dedicated to my parents,*

*Qing-Yan Chen and Men-lan Shaw, my sister Chia-Yu (Christy) Chen,*

*and my beautiful fiancée Yu-Jung (Ruby) Lin,*

*for their encouragement, support and, love.*

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Why so disturbed within me?

Put your hope in God,

for I will yet praise him,

my Savior and my God.

-Psalm 42:5

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# LIST OF SYMBOLS AND ABBREVIATIONS

| | |
|---|---|
| ARC | Anti-reflection coating |
| BSF | Back surface field |
| $BSRV$ | Back surface recombination velocity |
| CAD | Computer aided design |
| CVD | Chemical vapor deposition |
| epi-Si | Epitaxially grown Si |
| EpiWE | Epitaixal wafer equivalent |
| $\eta$ | Efficiency |
| $FF$ | Fill factor |
| FCA | Free carrier absorption |
| FSF | Front surface field |
| HAE | Highest achievable efficiency |
| HLI | High level injection |
| $J_o$ | Saturation current density |
| $J_{oe}$ | Emitter saturation current density |
| $J_{oe.metal}$ | Metal contribution of $J_{oe}$ |
| $J_{oe.field}$ | Passivated field contribution of $J_{oe}$ |
| $J_{ob}$ | Base saturation current density |
| $J_{ob.bulk}$ | Bulk contribution of $J_{ob}$ |
| $J'_{ob.metal}$ | Metal contribution of $J_{ob}$ |
| $J'_{ob.field}$ | Passivated field contribution of $J_{ob}$ |
| $J'_{ob}$ | BSF contribution of $J_{ob}$ |
| $J_{sc}$ | Short-circuit current density |
| LFC | Laser fired contact |

| | |
|---|---|
| LID | Light induced degradation |
| LLI | Low level injection |
| $N_s$ | Surface concentration |
| PV | Photovoltaic |
| PSI | Porous Si |
| PERC | Passivated emitter and rear cell |
| PERL | Passivated emitter, rear locally-diffused |
| PERT | Passivated emitter, rear totally-diffused |
| PL | Photolithography |
| $P_{in}$ | Input power |
| PSG | Phosphosilicate glass |
| Poly-Si | Polycrystalline Si |
| PVD | Physical vapor deposition |
| $R_s$ | Series-resistance |
| $R'_s$ | $R_s$ contribution from front contact, fingers and busbars |
| $R_{sh}$ | Shunt-resistance |
| $R_b$ | Back internal reflectance |
| SIPOS | Semi-Insulating Polycrystalline Silicon |
| SRH | Shockley-Read-Hall recombination |
| SRV | Surface recombination velocity |
| $S_{eff}$ | Effective back surface recombination velocity |
| TOPCon | Tunnel oxide passivated contact |
| $\tau_{bulk}$ | Bulk lifetime |
| $\tau_{eff}$ | Effective lifetime |
| $V_{oc}$ | Open-circuit voltage |
| $v_n$ | Electron velocity |
| $v_p$ | Hole velocity |

| | |
|---|---|
| X | Sun |
| 2-layer-epi PERT | Epi-grown base and BSF PERT solar cell |
| 3-layer-epi PERT | Epi-grown emitter, base and BSF PERT solar cell |

# SUMMARY

Fossil fuels have been the dominant source of energy, which account for more than 80% of the world energy production today. However, fossil fuels are limited in supply and harmful to the environment due to pollution and emission of greenhouse gases. Photovoltaic (PV) provides an attractive and sensible alternative to fossil fuels as it directly converts sunlight into electricity without any undesirable impact to the environment. In addition, sunlight, which is the fuel for solar cells, is free, not localized and essentially unlimited. However, solar PV only accounts 0.4% of total electricity generation in United States in 2014 because of the higher cost compared to fossil fuels.

Cost analysis shows that 30-33% of the cost of a finished solar module is attributed to Si wafer. Therefore, solar module price can be reduced substantially by lowering the material cost or reducing its use by increasing cell efficiency. This provided the motivation in this research to achieve high efficiency low-cost commercial ready screen-printed Si solar cell by reducing material cost and raising cell efficiency. Two specific solutions to material cost reduction are implemented in the thesis: low to medium concentrator (2-20 suns) Si solar cell which reduces the required cell area by a factor of concentration ratio, and the use of epitaxially grown Kerfless Si (epi-Si) wafers which eliminates the need for polycrystalline silicon (Poly-Si) feedstock, ingot growth, and wafer slicing. In addition, significant emphasis is placed in this thesis on modeling, design, technology innovation, and fabrication of high efficiency commercial size Si cells to reduce the cost ($/Wp) of PV module.

In Chapter II, the fundamental solar cell physics is reviewed. Chapter III reviews the literature pertaining to each task in this thesis.

Concentrator PV provides a unique opportunity to lower the cost of solar electricity. In a concentrator PV system, the expensive semiconductor material is replaced by less expensive optics while providing the same or even more power. The use of low to medium concentrator system with high efficiency screen-printed Si solar cells provides a path to attain grid parity since it has the right combination of cost and efficiency. However, there is a need to understand and modify the current screen-printed 1 sun (1X) Si cell to achieve higher efficiency under low to medium concentration. Therefore, Chapter IV (Task 1) deals with device modeling and a methodology to modify 1X screen-printed cells to achieve high efficiency under different concentration. The model is then validated by fabricating high efficiency metal paste printed cells. The detailed modeling in Chapter IV shows that the Highest Achievable Efficiency (HAE) at any given concentration is a function of metal paste, contact parameters, and grid pattern. These started with $\sim$18.3% efficient baseline 1X Si solar cells and its efficiency was raised to >20% by concentrator grid design. Consistent with the model calculations, metal screen-printed cells were fabricated using $\sim$110 $\mu$m wide 70 mm long fingers with 1.37 mm spacing as opposed to 2.3 mm spacing in 1X cells. These cells gave an efficiency of 18.9% at 4X. The cell efficiency was then improved to 19.0% at 4-5X with 1.63 mm finger spacing and shorter finger length (25 mm of effective finger length). In addition, 50 $\mu$m wide direct extrusion printed fingers were applied with 0.75 mm spacing which resulted in >20% efficient cells in the concentration range of 3-16X. Finally, a technology roadmap to achieve $\geq$21% efficient concentrator cells was developed in Chapter IV by using more advanced cell structures. The methodology developed and used in this task provided excellent guidelines for designing grid patterns to achieve maximum efficiency under low to medium concentration for any given cell design.

Chapters V to IX (Task 2 to 5) in this thesis deal with solar cells made on epitaxially grown Si (epi-Si) wafers with different structures to reduce the Si material cost.

Compared to the traditional Si wafer technology, the epi-Si wafer technology has the ability to by-pass the three costly process steps: growth of high purity Poly-Si by Siemens process using trichlorosilane gas, ingot growth by Czochralski process and wafer dicing which results in >40% loss of Si in the form of dust (Kerf loss). The epi-Si wafers can be directly grown on a substrate by Chemical Vapor Deposition (CVD) using chlorosilanes. In Chapter VI (Task 2), epi-Si cells were made using epitaixal wafer equivalent (EpiWE) structure, which involves eptiaxially grown Si active layer on top of a thin porous Si (PSI) formed anodically an a highly doped low-cost Si substrate. The PSI layer in between the active epi-Si layer and low cost substrate was engineered in this thesis to be a good back reflector. Guidelines were established for refractive index and thickness of PSI to enhance the back reflection. A standard industrial cell process was applied on this kind of EpiWE wafer (182 $cm^2$ large and 90 $\mu$m thick epi-Si active layer on top of PSI and low-cost substrate). Cell efficiency of 17.3% was demonstrated on thin $\leq$90 $\mu$m epi-Si active layer, which was the best in class at the time.

Since Si substrate was part of the EpiWE cell structure, full benefit of Kerf loss saving could not be realized from this epi-Si solar cell structure. To overcome this problem, in Chapter VII (Task 3), thin epi-Si cells were fabricated using a layer transfer process to a glass/EVA carrier so that the Si substrate can be reused for next epi-Si growth. An epi-Si based technology from these epi-grown wafers to solar cell module is demonstrated in this task, which can greatly reduce Kerf loss because of the reuse of the Si substrate. This concept involved forming PSI layer on a reusable Si substrate to not only grow but also exfoliate and transfer thin epi-Si active layer to a glass/EVA structure as opposed to Chapter VI (Task 2) where the PSI layer served as a back reflector in between the substrate and epi-Si was an integral part of EpiWE cell structure. Process yield was challenged in this task initially because of the exfoliation process, but was solved later by use of a sealed edge wafer structure, optimization of

texturing process, and a low temperature laser fired local Al contact process. High efficiency of 17.2% was achieved on thin (90 $\mu$m) large-area (156 cm$^2$) epitaxially grown and layer transferred Si wafers with screen-printed contacts and tabs under EVA/glass encapsulation. This is equivalent to $\sim$18.0% efficiency in air, assuming $\sim$5% encapsulation loss due to reflectance and resistance in a module configuration. Also, cell efficiency of 15.6-17.2% was demonstrated using 40-90 $\mu$m thick epi-Si layers under EVA/glass. This is the first time such thin and large area epi-Si cells were demonstrated using layer transfer technology in combination with industrial type screen-printed front contacts.

Although some good efficiency numbers were realized on the above thin ($\leq$90 $\mu$m) epi-Si solar cells, the module assembly posed additional challenges for low-cost PV modules. Therefore, in Chapter VIII (Task 4), we undertook the development of large-area free-standing high efficiency screen-printed epi-Si cells on thicker (120$\sim$180 $\mu$m) epi-Si wafers made by layer transfer process. Currently, $\sim$180 $\mu$m thick Si wafers are used for mass production. Therefore, these thick epi-Si wafers can be directly used by PV manufacturers because rest of the cell processing is identical to the traditional crystalline Si solar cells. The challenge was to achieve equal or higher efficiency from epi-Si wafers so that the full benefit of wafer cost reduction can be realized. Minority carrier lifetime of these epi-Si wafers was initially inferior to commercial Cz wafers, but during the course of this research, our collaborator Crystal Solar was able to improve it and make it comparable to Cz wafers. Close to 20% cell efficiency was achieved in Chapter VIII using the industrial type process sequence in combination with advanced PERC and PERT cell structures on p-type and n-type epi-Si wafers, respectively.

It is important to recognize that doping level can be precisely controlled by the dopant gas during the epitaxial growth of Si. Therefore, the emitter and Back Surface Field (BSF) doped regions can be epitaxially grown at the same time as the bulk

wafer to further simplify the solar cell fabrication and reduce the number of processing steps. Our device modeling in Chapter IX (Task 5) shows that, besides cost, even higher efficiency can be achieved with epitaxially grown emitter/BSF regions with superior doping profiles compared to traditional heavy diffusion profiles used in industry today. This is because much deeper and lightly doped regions can be formed by epi-growth, which reduces Auger recombination and improves surface passivation to lower $J_o$. In addition, lower sheet resistance can be achieved with this deep and lightly doped epi-grown emitters, which can reduce shadow losses by reduced metal coverage. Therefore, in Chapter IX, we modeled and fabricated cells to demonstrate the benefit of epi-grown $p^+$ layer on p-type solar cells. First, Sentaurus 2D device model was used to assess the impact of the epi-grown $p^+$ layer, which showed an efficiency gain of ∼0.5% for PERT (passivated emitter, rear totally-diffused) structure over the traditional PERC (passivated emitter and rear cell) cell with local $p^+$ BSF. This was validated by the cell fabrication which showed an efficiency of ∼20.1% for the PERC device on p-type epi-Si wafer and ∼20.3% for the PERT cell on $pp^+$ epi-Si substrate. To demonstrate the value of built-in epi-Si junctions, a $n^+pp^+$ three-layer-epi PERT cell with epi-grown emitter, base and BSF is proposed and modeled. It is shown that screen printing of 40 $\mu$m wide lines in combination with thin floating busbars and improved bulk material properties can raise the cell efficiency to >22.7%. Thus epi-Si technology with built-in junctions has the potential of not only reducing wafer cost but also giving higher cell efficiency compared to the traditional Cz wafers used in industry today.

In order to achieve the highest cell efficiency, the recombination loss in the entire cell needs to be minimized. Current industry cell performance is largely limited by metal and doped region recombination. In Chapter X (Task 6), we have studied and modeled passivated contacts which can reduce or eliminate above recombination and give much higher $V_{oc}$ and efficiency. This is accomplished by inserting a thin

dielectric between the Si wafer and doped/metallized regions. The contacts have been shown to be very conductive (small series resistance) and carrier selective (allow tunneling or flow of majority carriers easily while blocking the flow of minority carriers). Since metal and doped regions are not in direct contact with the absorber, their contribution to $J_o$ is virtually eliminated. Using this concept, a joint program between GT (Georgia Institute of Technology), Fraunhofer ISE (Fraunhofer Institute for Solar Energy System ISE), and NREL (National Renewable Energy Laboratory) has produced 24.9% efficiency on a small area (4 $cm^2$) laboratory cell on Fz Si with photolithography front contacts. Exact modeling and theory of these cells is still not fully understood. In Chapter X, we developed a methodology for modeling Tunnel Oxide Passivated Contact (TOPCon) cells and applied it to establish the efficiency potential of this concept for large area manufacturable screen-printed cells. Chapter X shows the development of the methodology for modeling such cells and its validation by accurate modeling of the 24.9% TOPCon cell fabricated by Fraunhofer ISE. This methodology involves replacing the TOPCon region on the back by carrier selective electron and hole recombination velocities to match the measured dark saturation current density ($J'_{ob}$) of the TOPCon region as well as all the light IV parameters of the TOPCon cell. The modeling is then extended to assess the efficiency potential of large area TOPCon cell on commercial grade n-type Cz material with conventional screen-printed front contact on boron doped emitter. To use realistic input parameters, a 21% n-type PERT cell was fabricated using the manufacturable technologies with 90 Ω/sq homogeneous emitter and 5 Ω-cm 1.5 ms lifetime base. Device modeling showed that if the back of this cell with fully diffused $n^+$ region and local metal contacts is replaced by the TOPCon structure (1.5 nm tunnel oxide capped with full area $n^+$-Poly-Si layer and metal with $J'_{ob}$ $\leq$8 fA/$cm^2$), the cell efficiency would increase to only $\sim$21.6% because the performance is limited by the recombination in emitter.

Detailed modeling is performed to show that the implementation of a selective emitter (150/20 Ω/sq) can raise the efficiency of TOPCon Cz cell to ∼22.6%. Finally, modeling is extended to show that ∼23.2% efficiency can be achieved by this single side TOPCon Cz cell structure with screen printing of 40 $\mu$m wide lines, floating busbar, and 10 Ω-cm wafers with 3 ms lifetime.

In Chapter XI, all the know-how developed in the thesis was combined to provide guidelines for next generation low-cost high-efficiency cells using advanced cell structures. It is shown that by combining TOPCon concept with epi-grown emitter can lead to ∼23.4% cell efficiency. Finally, it is shown that optimum grid design of the 23.4% TOPCon epi-Si cell can raise the efficiency to ∼24.5% at 4X concentration.

This work has resulted in over 11 publications in peer-reviewed journals, international refereed conferences and workshop proceedings. The research in this thesis was supported by Incubator Project with Crystal Solar, FPACE, Solarmat I, FPACE II, and Solarmat II funded by U.S. Department of Energy.

# CHAPTER I

# INTRODUCTION

## *1.1 Statement of the Problem*

The demand for energy has been growing rapidly for the past 40 years as reflected in the steady growth world energy supply in Figure 1 [1]. Figure 1 also shows that fossil fuels (coal, oil and natural gas) have been the main source of energy, which account for more than 80% of the world energy production today. However, fossil fuels are limited in supply and harmful to the environment due to pollution and emission of greenhouse gases, which are the main cause of global warming and climate change. This problem

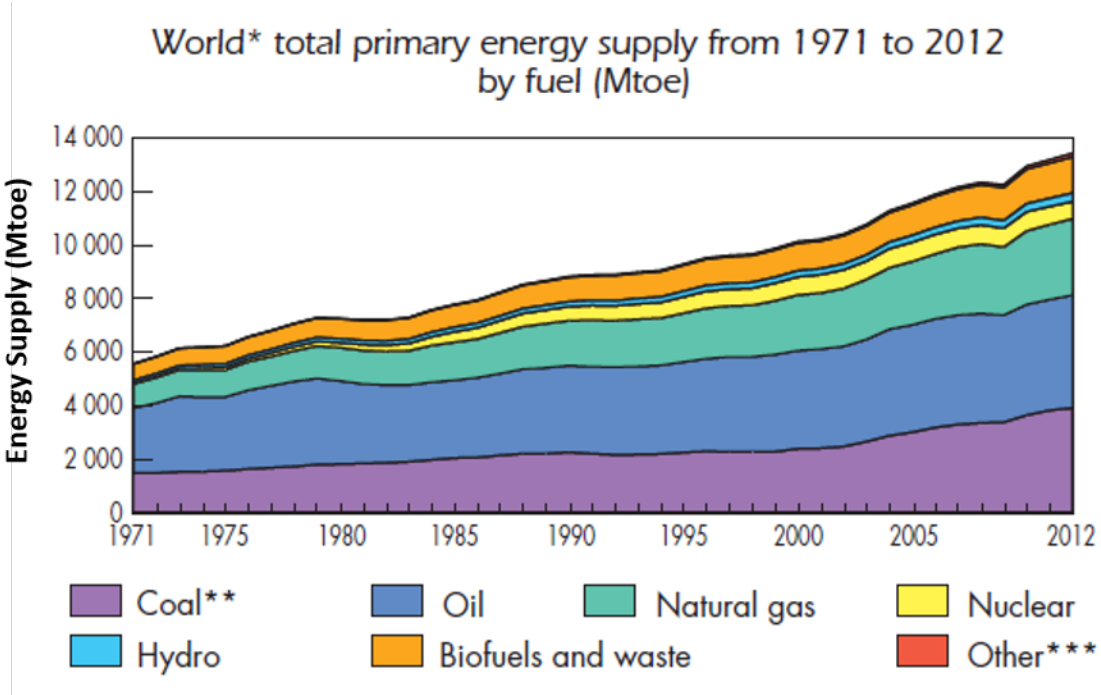



**Figure 1:** World total primary energy supply from 1971 to 2012 by fuel (Mtoe). 1 tonne of oil equivalent (toe) = 11.63 megawatt hours.*World includes international aviation and international marine bunkers. **In these graphs, peat and oil shale are aggregated with coal. ***Other includes geothermal, solar, wind, heat, etc [1].

can be partly solved by replacing fossil fuels with nuclear power. However, the nuclear power introduces the challenge of heat dissipation, radioactive waste disposal, and safety, as evidenced by Three Mile Island accident in 1979, Chernobyl disaster in 1986, and Fukushima Daiichi nuclear disaster in 2011.

Therefore, renewable energy sources listed in Figure 2 provide an attractive and sensible alternative to fossil fuels and nuclear power for the growing energy and electricity demand. Among all the renewable alternatives, Photovoltaic (PV) is particularly attractive because it converts sunlight into electricity without any undesirable impact on the environment. In addition, sunlight, which is the fuel for solar cells, is free, not localized and essentially unlimited. Nevertheless, PV only accounts very little of the world energy portfolio (Figure 1) because of the higher cost compared

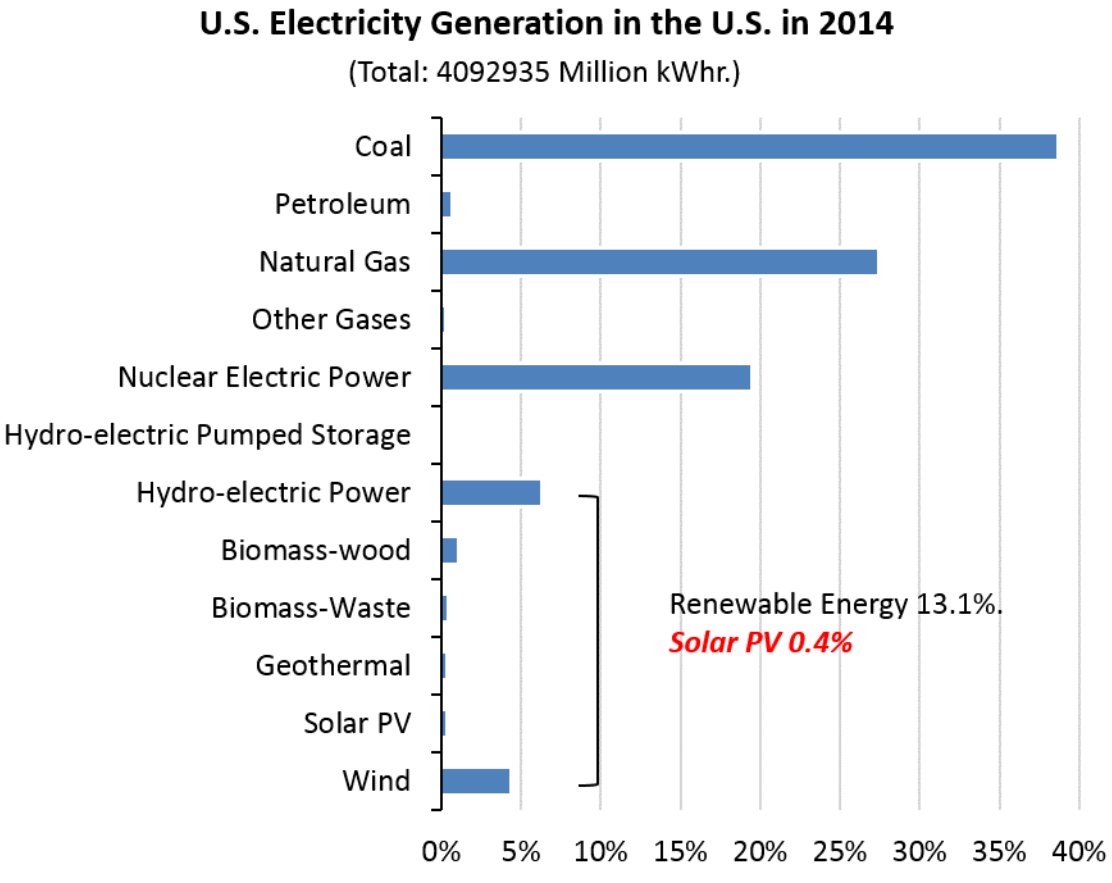



**Figure 2:** Various sources of electricity generation in the U.S. in 2014 [2].

to fossil fuels and nuclear power. Figure 2 shows that only 0.4% of total electricity generation is from solar PV in United States in 2014.

Figure 3 shows the learning curve for module price ($/Wp) as function of cumulative PV module shipments (MWp) [3]. Every time we double the total amount of installed PV in the world, the PV module price drops by ∼20%. This has brought PV within the striking distance of grid parity with fossil fuels and in many parts of the world it is even below the cost of fossil fuels. This is the result of economy of scale, technology, innovation, policies and incentives promoting PV around the globe. In 1976, the PV module price was ∼100 $/Wp with cumulative PV module shipment of 0.4 MW. However, by 2014, module price decreased by more than a factor of 100 to ∼0.62 $/Wp with cumulative PV module shipment reaching 184 GWp (Figure 3)

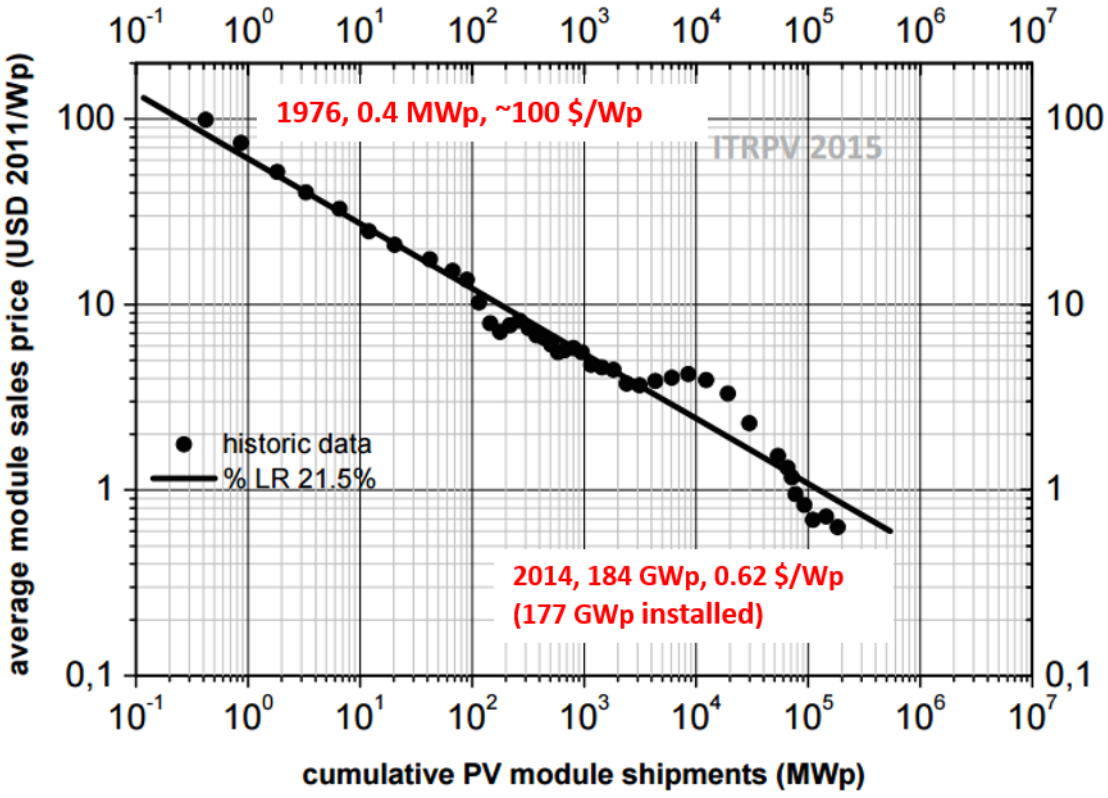



**Figure 3:** The learning curve for module price as function of cumulative PV module shipments [3].

and annual module shipment of 39.3 GW. Even more impressive is the fact that PV accounted for 40% of new electricity generation capacity in the US in the first half of 2015 [4]. Today, PV can produce electricity at ∼12 ¢/kWh in Atlanta, USA without incentives. U.S. Department of Energy Sunshot Program goal is to reduce this to 6 ¢/kWh by 2020. In order to reach global grid parity of ∼6 ¢/kWh, further price reduction and technology innovation is necessary.

Figure 4 shows that 30-33% of the cost is attributed to Si wafer in a finished solar module in 2013-2015 [3]. Therefore, solar module price can be reduced substantially by lowering the material cost and reducing its use by increasing cell efficiency. This provided the motivation in this research to achieve high efficiency low-cost commercial ready screen-printed Si solar cells with reduced material cost. Two specific solutions to material cost reduction are implemented in the thesis: low to medium concentrator

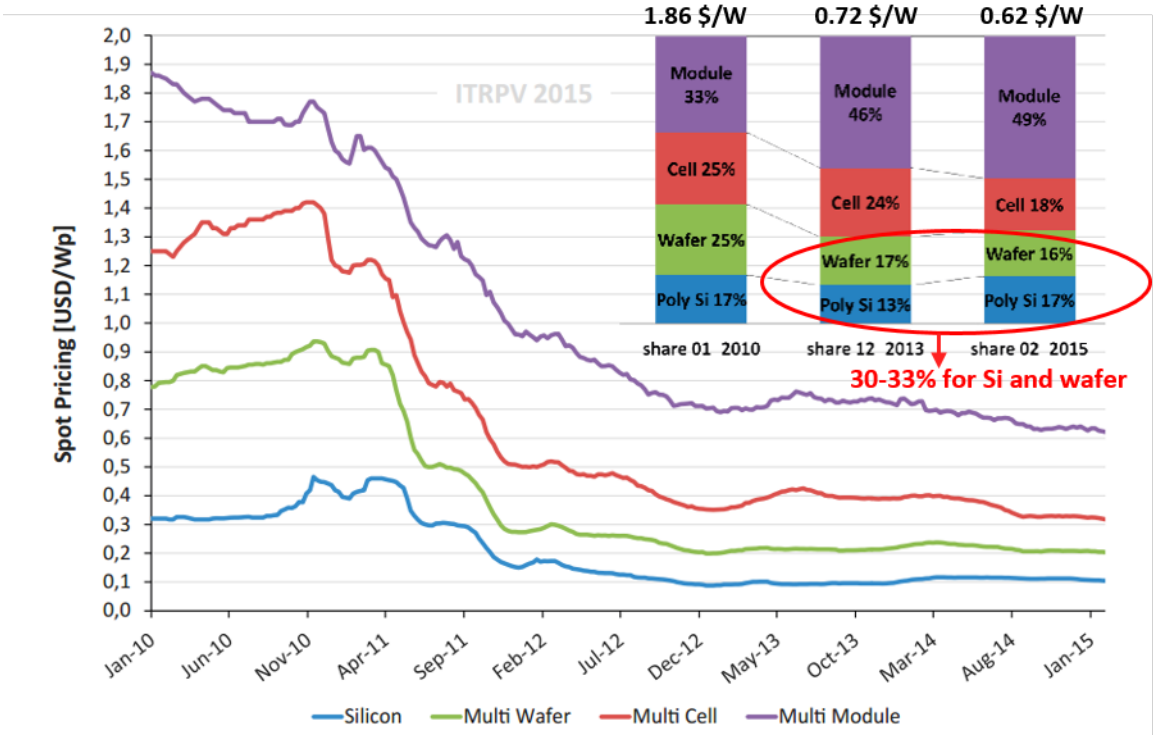



**Figure 4:** Price trends for Poly-Si, mc-Si wafers, cells, and c-Si modules, with assumptions of 44.1 wafers per kg (∼22.7 g/wafer) and average mc-Si cell efficiency of 17.3% (4.21 Wp) [3].

(2-20 suns (X)) Si solar cell which reduces the required cell area or number of cells by a factor of concentration ratio [5], and the use of epitaxially grown Kerfless Si (epi-Si) wafers which eliminates the need for Poly-Si feedstock, ingot growth and wafer slicing which leads to >40% loss of Si in the form of Si dust [6]. In addition, significant emphasis is placed in this thesis on modeling, design, technology innovation, and fabrication of high efficiency Si cells to further reduce the cost ($/Wp) of PV module.

## *1.2 Specific Research Objectives*

### 1.2.1 Task 1: Development of High Efficiency Screen-printed Low-Medium Concentrator Si Solar Cell

Concentrator PV provides a unique opportunity to lower the cost of solar electricity since it replaces expensive semiconductor material by less expensive optics while providing the same or even higher cell efficiency [5]. Concentrator systems can be divided into three categories based on their concentration ratio: high concentrator system (larger than 100X), medium concentrator system (10-100X), and low concentrator system (smaller than 10X). Currently, the highest reported efficiency of a multi-junction concentrator solar cell using very expensive III-V materials and process technologies has reached ∼44.4% at 302X [7]. However, high concentrator systems have several drawbacks: (a) need for accurate tracking system because of smaller acceptance angle, (b) more expensive heat dissipation system due to high operating temperature, and (c) more expensive cells produced on extremely expensive III-V materials by lower throughput MOCVD or MBE techniques compared to screen-printed Si solar cells studied in this thesis.

The use of low to medium concentrator system with higher efficiency (∼20%) screen-printed Si solar cells can achieve the right combination of cost and efficiency to attain grid parity. The cost of the optics for such systems is cheaper than single crystal Si [8]. Since the concentration ratio is low (10-20X), the tracking and heat dissipation systems are much simpler and less expensive [9]. However, there is a real

need to understand and modify the 1 sun Si cell structure and design to achieve highest efficiency at low to medium concentration without adding appreciable cost. This is because low-cost screen-printed contacts are not as good and sophisticated as the expensive photolithography contacts in terms of shading and contact resistance. Both these factors are critical for achieving high efficiency concentrator cells.

Therefore, in Task 1, a methodology is established to model and modify 1 sun (1X) screen-printed cells to achieve high efficiency under low to medium concentration. A systematic approach is proposed to calculate the highest cell efficiency under desired concentration or illumination based on screen-printed grid design, contact parameters and cell technologies. Following the guidelines of this fundamental study and modeling, high efficiency paste-printed concentrator Si solar cells were fabricated under 3-16X concentration with 50 $\mu$m wide contact fingers. Finally, $\geq$21% efficient low-medium concentrator Si solar cell was modeled with more advanced cell structures.

### 1.2.2 Task 2: Development of Screen-printed Thin Epi-Si Solar Cell using Epitaxial Wafer Equivalent Structure

Currently, most Si solar wafers are fabricated by the process shown in Figure 5, which involves three very high temperature crystallization processes that consume lot of energy and increase cost. Then there is cost associated with growing Si ingots from Poly-Si feedstock. Finally, the wafer dicing from the ingot results in >40% loss of Si in the form of Si dust (Kerf loss). This provided the motivation in this research to investigate epitaxially grown Si wafers to by-pass the all three costly process steps (Figure 5) used in manufacturing traditional Si wafers: growth of high purity Poly-Si by Siemens process, ingot growth by Czochralski process and wafer dicing or wire saws. The epi-Si wafers used in this task are directly grown on a substrate by Chemical Vapor Deposition (CVD) using chlorosilanes ($SiHCl_3$, $SiCl_4$, $SiH_2Cl_2$) gases. The epi-Si wafer technology can be roughly divided into two groups:

Epitaxial Wafer Equivalent (EpiWE) and Porous Si (PSI) Layer Transfer processes. Both concepts are studied in the thesis and described in more details in Chapter III.

In Task 2, high efficiency epi-Si cells using Epitaxial Wafer Equivalent (EpiWE) structure and Porous Si (PSI) back reflector were modeled, studied, and fabricated. PSI layer was grown between the Si substrate and the epi-grown thin wafer (<100 $\mu$m) to serve as a back reflector. In this task, PSI was optimized to form an efficient back mirror for the thin epi-Si cells to enhance current and cell efficiency. High efficiency large area screen-printed thin epi-Si solar cell using EpiWE cell structure with PSI back reflector were fabricated by standard low cost Si cell process sequence. Detailed device modeling was performed to demonstrate the efficiency potential of very thin (10-30 $\mu$m thick) epi-Si cell structure with excellent PSI reflector. Note that the PSI layer can be also used for exfoliation or separation of the epi-Si layer from the reusable substrate by a mechanical treatment. However, in this task, epi-Si layer was not lifted off from the substrate but the substrate remained part of the finished EpiWE cell.

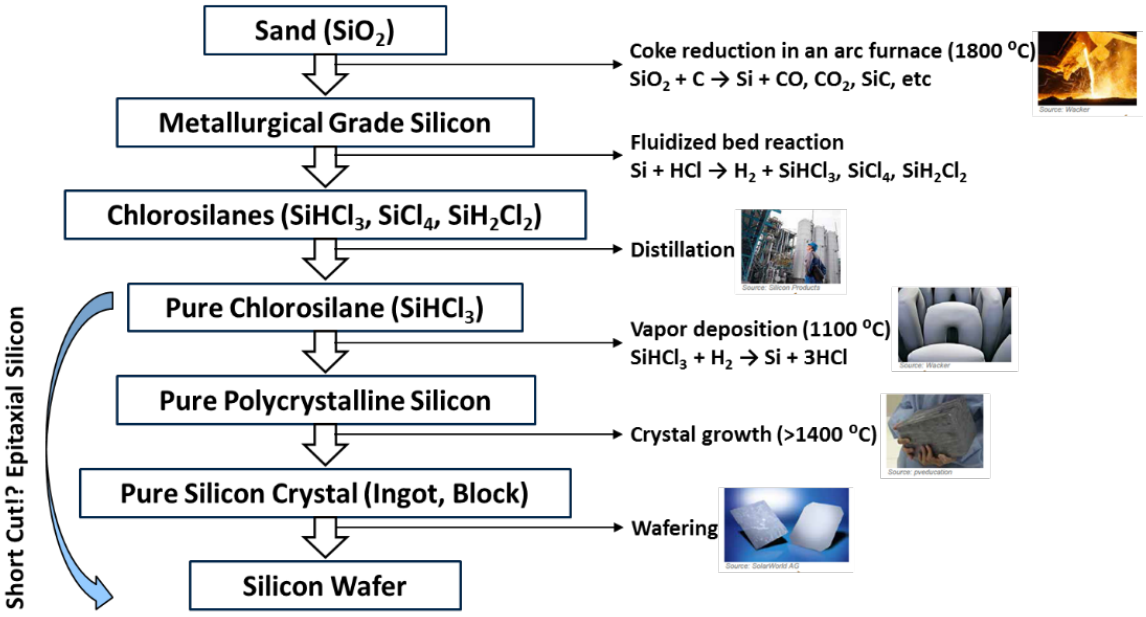



**Figure 5:** Traditional process flow for silicon solar wafers beginning from sand. Epi-Si wafer technology can greatly simplified the process from chlorosilanes directly to Si wafer.

### 1.2.3 Task 3: Development of Screen-printed Thin Epi-Si Solar Cell using Porous Si Layer Transfer Process

Since Si substrate was part of the EpiWE cell structure in Task 2, Kerf loss saving could not be fully realized in that approach. In an effort to avoid the Kerf loss, a layer transfer process was introduced in Task 3 in order to re-use the Si substrate. This involved fabrication of the front side of large area screen-printed high efficiency cells on 40-90 $\mu$m thick epi-Si wafers grown on the reusable substrate. During the front side processing, the substrate was part of the structure so that thin epi-Si layer can be handled without breakage. After that, the wafers were laminated with tab and glass/EVA followed by a layer transfer process. The epi-Si wafer was exfoliated from the substrate by a mechanical treatment and attached to a glass/EVA carrier on the front side to finish the back side of the thin cell. A low temperature laser process was used to form local contacts on the back side to finish the device. Glass/EVA carrier on the front is used as part of the module assembly. This approach (from wafer to module) combines the use of thin Kerfless epi-Si wafer and conventional low-cost screen-printed technology.

### 1.2.4 Task 4: Development of Screen-printed Epi-Si Solar Cell on Free-standing Epi-Si Kerfless Wafer

Although reasonably good efficiency was achieved on thin epi-Si wafers using layer transfer process in Task 3, the exfoliation and module assembly complications posed additional challenges and steps for low-cost manufacturing of PV modules. Since epi-Si wafer quality is often lower than Cz because of potential contamination, thick epi-Si wafers have not been used for cells. However, our collaborator Crystal Solar has recently improved the epi-Si wafer quality significantly, which provided the motivation to make high efficiency cells on thicker epi-Si wafer (120-180 $\mu$m) to explore the potential of this Kerfless technology. Therefore, in Task 4 we undertook the development of large-area free-standing high efficiency screen-printed epi-Si cells on

thicker (120∼180$\mu$m) epi-Si wafers made by layer transfer process. Both p-type and n-type high efficiency screen-printed cells were fabricated in order to demonstrate the material quality and manufacturability of the thick epi-Si wafers, which can save up to 50% of wafer cost compared to standard Cz technology [6]. Finally, in this task, device modeling was used to establish the material requirements for resistivity and lifetime to achieve >20% efficient cell using the current low-cost Si cell processing technologies.

### 1.2.5 Task 5: Development of Advanced High Efficiency Large Area Screen-printed Solar Cell on Direct Kerfless Epitaxially Grown Mono-Crystalline Si Wafer

It is important to recognize that doping level can be precisely controlled by the dopant gas during the epitaxial growth of Si. Therefore, the emitter and Back Surface Field (BSF) regions can be grown at the same time as the base to further simplify the solar cell fabrication. In addition, device modeling in this task shows that cell with even higher efficiency can be achieved for epitaxially grown emitter/BSF than the traditional diffused emitter/BSF because much deeper and lighter doped region can be formed by epi-Si without compromising the passivation and sheet resistance. As a result, in Task 5, we first modeled the p-type PERT (passivated emitter, rear totally-diffused) cell with different BSF profiles and show that a uniform lightly doped deep (15 $\mu$m, $5 \times 10^{17}$cm$^{-3}$) BSF can improve the cell performance by ∼0.5% compared to the counterpart PERC (passivated emitter and rear cell) solar cell with local BSF. Following the guidelines of the model, PERT solar cells were fabricated from epi-grown pp$^+$ structures with built-in full area BSF along with PERC cells with local BSF on Cz and epi-grown p-type wafers for comparison. Finally, detailed device modeling was performed in this task to show the efficiency potential (>22.7%) of a three layer epi-grown PERT cell with selective emitter formed on carefully designed epitaxially grown emitter, base and BSF structure.

### 1.2.6 Task 6: Modeling the Potential of Next Generation Screen-printed N-type Front Junction Cz Si Solar Cells with Tunnel Oxide Passivated Back Contact

In order to achieve the highest cell efficiency, the recombination loss in the entire cell needs to be minimized. The 25% efficient PERL (passivated emitter, rear locally-diffused) cell fabricated at UNSW [10, 11] is a great example that implemented excellent front and back surface passivation by thermal oxidation, reduced metal recombination by photolithography contacts and selective doping with highly diffused regions underneath the contacts, and reduced bulk recombination by the use of high lifetime Fz material. However, even this PERL cell suffers from the recombination loss due to local metal contacts and highly doped regions in the absorber material. That is why the $V_{oc}$ of the PERL cell is only ∼706 mV with total recombination or saturation current density ($J_o$) of ∼50 fA/cm$^2$. A Tunnel Oxide Passivated contact (TOPCon) [12], where a ∼1.5 nm thick tunnel oxide is used to displace doped Poly-Si and metal regions outside the absorber, should help reduce the $J_o$ and give much higher $V_{oc}$. Fraunhofer ISE has recently demonstrated small area (4 cm$^2$) 24.9% efficient cells on Fz Si with $V_{oc}$ of 718 mV and $J_o$ of ∼30 fA/cm$^2$ by using Photolithography (PL) contacts, boron doped selective emitter on the front, and TOPCon on the back [13]. This task first shows a methodology for cell modeling and its validation by matching the 24.9% TOPCon cell. The 2D device modeling is then extended to calculate the efficiency potential of a more manufacturable TOPCon cell on commercial grade Cz material with passivated contact on the back and traditional screen-printed front contacts on boron implanted front emitter. Besides developing the roadmap to ≥23% manufacturable TOPCon cells, in this task, the individual impact of high quality Cz material (10 Ω-cm resistivity and 3 ms lifetime), lateral minority carrier transport in the base, and fine line (40 $\mu$m) metallization were also quantified.

Finally, all the research and knowledge developed in this thesis is utilized to model

highest achievable and manufacturable cell efficiency cell from epitaxially grown structures to provide directions for future research. It is predicted that ∼23.4% efficiency is possible with epi-grown $p^+n$ structure with lightly doped deep $p^+$ field emitter on n-type base, $p^{++}$ selective emitter on the front, and n-type TOPCon on the back. The process flow for such a cell is also proposed. In addition, the model is extended to calculate the cell efficiency from such a device under low-medium concentration.

# CHAPTER II

# PHYSICS OF SOLAR CELL

## *2.1 Basic Solar Cell Operation*

A solar cell is a device that converts light into electricity. Usually, it has a p-n junction in the semiconductor material, as shown in Figure 6. When the sun light strikes a solar cell, electron and hole pairs are generated if the light energy is greater than the semiconductor band gap. These pairs are separated into electrons and holes by the built-in electric field at the junction. The electrons then flow into an external circuit to give electrical power.

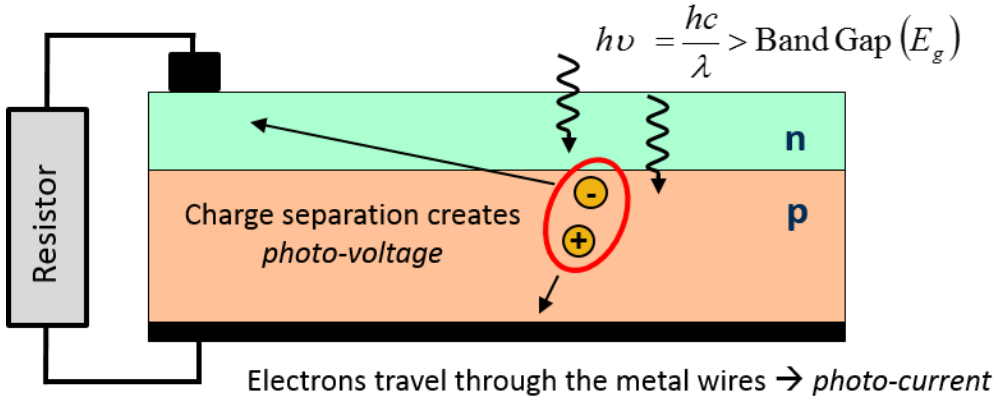



**Figure 6:** The cross-section of a semiconductor solar cell.

Figure 7 shows the IV curve of a solar cell. Three important parameters are used to characterize a solar cell: open-circuit voltage ($V_{oc}$), short-circuit current density ($J_{sc}$), and fill factor ($FF$). $V_{oc}$, is defined as the maximum voltage when the current is zero. Likewise, $J_{sc}$ is defined as the maximum current when the voltage is zero. $FF$ factor is defined as the ratio of the maximum power to the product of $V_{oc}$ and $J_{sc}$ (Figure 7). The cell efficiency ($\eta$) is defined as the product of $V_{oc}$, $J_{sc}$ and $FF$

divided by the input power ($P_{in}$). Therefore, the larger $V_{oc}$, $J_{sc}$ and $FF$, the better cell efficiency.

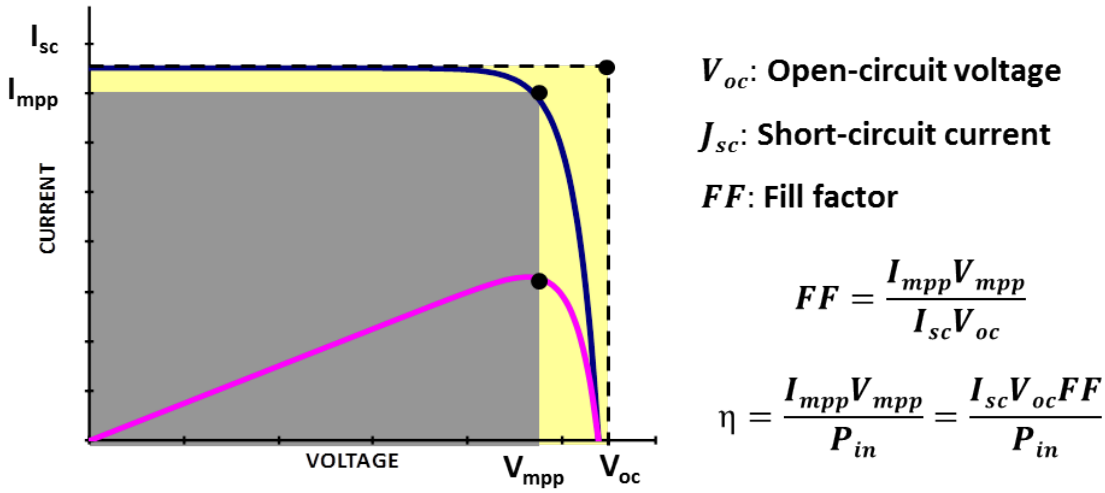



**Figure 7:** IV curve of a solar cell.

## *2.2 Losses Mechanisms in Solar Cell*

Since one of the objectives of this thesis is to model and fabricate high efficiency solar cells, it is important to understand and eliminate efficiency loss. Figure 8 shows different loss mechanisms in a solar cell, which can be divided into two groups: Optical and Electrical losses. Optical loss occurs because photons fail to generate electron and hole pairs, while electrical losses are associated with recombination and resistance.

### 2.2.1 Shading Loss

Usually, there are front and back contacts on a finished solar cell. The front grid contacts are made with metal and therefore create shadowing. Fewer and narrower grid lines reduce shading loss and increase $J_{sc}$. However, fewer grid lines increase resistive loss. Therefore, there is an optimum number of grid lines or fingers for a specific solar cell design or operating condition. This is as important part of this thesis since cells with different emitter design and sun concentration are studied. The

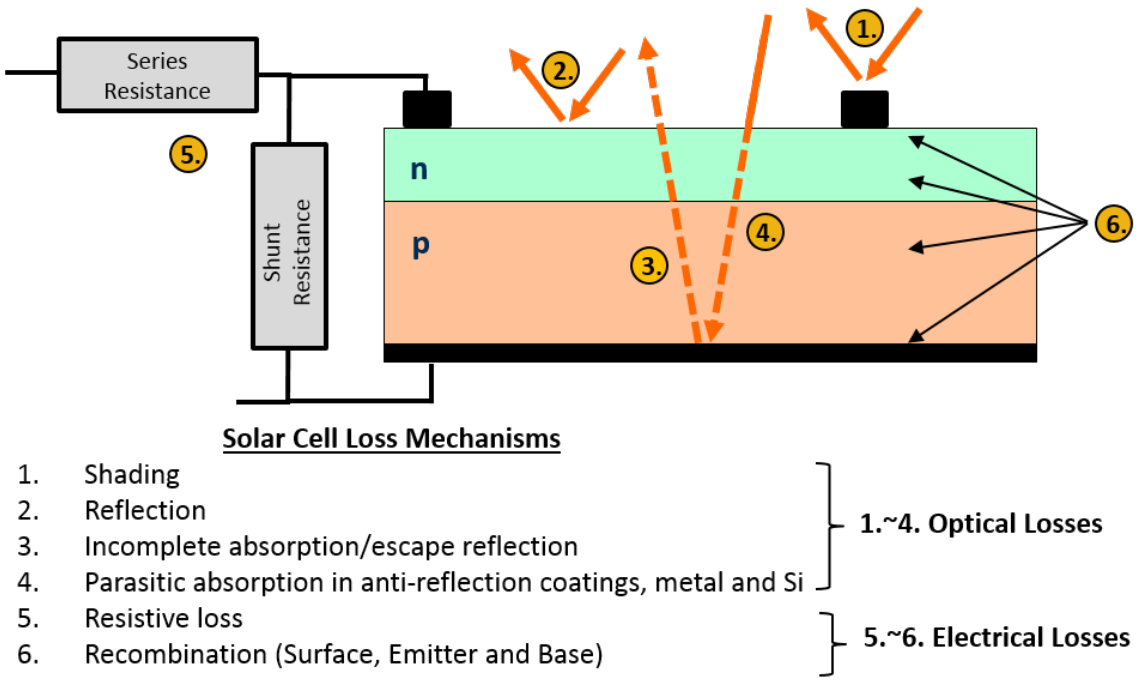



**Figure 8:** Loss Mechanisms in a solar cell.

trade off is discussed in more details in section 4.2 for low-medium concentrator Si solar cell.

### 2.2.2 Reflection Loss

In the non-metallized area between the grid lines, some light is reflected at the Air/Si interface and contributes to reflection loss. For a bare Si surface, about 30% of light is reflected. This loss is minimized by applying an anti-reflection coating (ARC) and

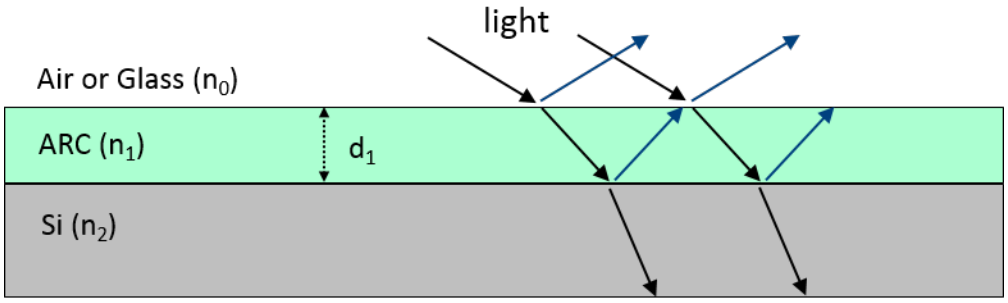



**Figure 9:** Anti-reflection coating on planar surface.

surface texturing, which can reduce this loss to <3%. Numerical ray tracing program, like Sunrays [14], is often used for calculation and minimization of this loss on ARC coated textured surface. Figure 9 shows the path of light on a planar surface coated with ARC. For a normal incident beam, the reflection value can be calculated using equation (1),where $\theta = \frac{2\pi n_1 d_1}{\lambda}$, $r_1 = \frac{n_0 - n_1}{n_0 + n_1}$, $r_2 = \frac{n_1 - n_2}{n_1 + n_2}$, where $n_0$, $n_1$, and $n_2$ are the refractive index of the air, ARC, and Si, respectively [5].

$$R = \frac{{r_1}^2 + {r_2}^2 + 2r_1 r_2 cos2\theta}{1 + {r_1}^2{r_2}^2 + 2r_1 r_2 cos2\theta} \tag{1}$$

The reflection is minimum when $n_1 d_1 = \frac{\lambda_0}{4}$ and $R_{min} = \left(\frac{{n_1}^2 - n_0 n_2}{{n_1}^2 + n_0 n_2}\right)^2$. $R_{min}$ is zero if the refractive index of ARC $n_1 = \sqrt{n_0 n_2}$. Thus an optimum ARC would require refractive index of 1.95 and thickness of 77 nm for $R_{min} = 0$ at $\lambda = 600$ nm.

### 2.2.3 Incomplete Absorption

Since Si is an indirect bandgap material, thick Si wafers (≥200 $\mu$m) are required for nearly full absorption. Figure 10 shows the absorption coefficient and absorption

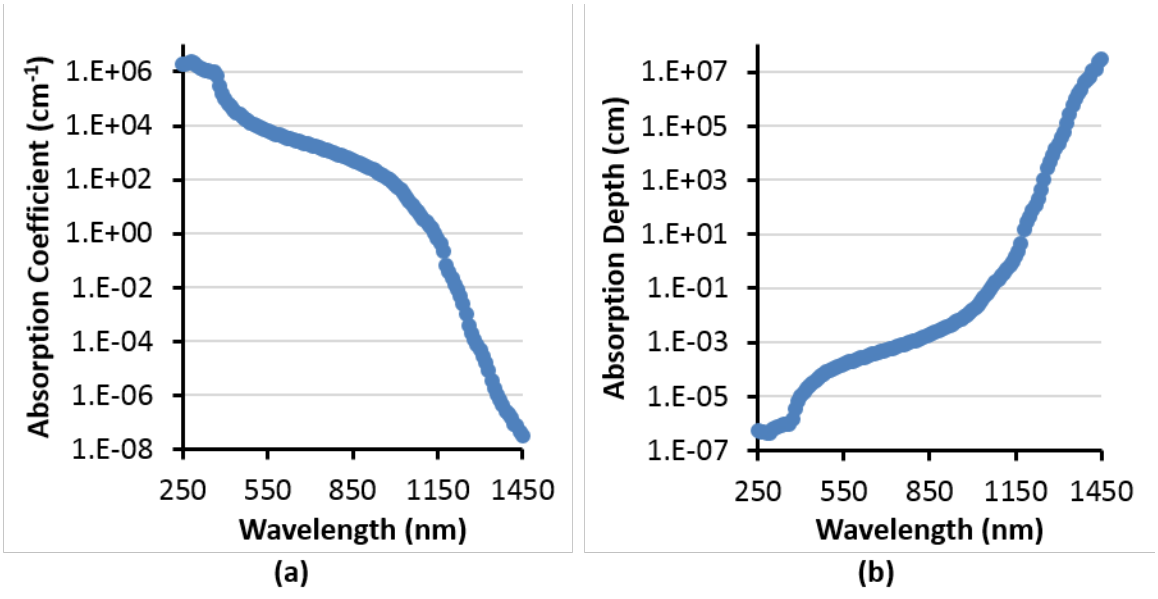



**Figure 10:** (a) Absorption coefficient of Si as function of wavelength. (b) Absorption depth in Si as function of wavelength

depth in Si [15]. In order to absorb long wavelength light (1000-1200 nm), few mm thickness of Si is needed. However, current Si solar cells are around 150-250 $\mu$m thick to minimize the cost. Therefore, long wavelength light is not absorbed in one pass through the Si wafer. A reflector (mirror) is needed on the backside to reflect the un-absorbed light back into the solar cell. In practice, >95% back reflectance is achieved currently in PERC cells [16] with the need of dielectric passivation capped with metal on the majority of the back surface. Back reflector design is done in this thesis (Section 6.1) using porous Si in-between the epi-grown Si and substrate.

### 2.2.4 Parasitic Absorption in Anti-Reflection Coatings, Metal and Si

Parasitic absorption can take place in ARC and metal contact in a solar cell. The light passing through a material is described by equation (2), where $I_0$ is the intensity of incident light, $I(x)$ is the intensity of light at depth $x$, and $\alpha$ is the absorption coefficient. The absorption coefficient is related to extinction coefficient, $k$, given by equation (3).

$$I(x) = I_0 e^{-\alpha x} \tag{2}$$

$$\alpha = \frac{4\pi k}{\lambda} \tag{3}$$

The smaller the $k$, the smaller the parasitic absorption in ARC. The ARC materials ($SiO_2$, $SiN_x$, etc) used in this thesis for Si solar cell have very low or zero $k$ in the 300-1200 nm wavelength range [17]. However, metals usually have relatively high $k$ [17]. Therefore, metal coverage should be minimized on the back.

Besides interband absorption in Si, Free Carrier Absorption (FCA) is an intraband absorption which becomes important at high carrier densities ($\geq 10^{18}$ cm$^{-3}$) and is described by equation (4) [18], where $\lambda$ is wavelength (nm).

$$\alpha_{FCA} = 2.6 \times 10^{-27} n\lambda^3 + 2.7 \times 10^{-24} p\lambda^2 \tag{4}$$

### 2.2.5 Resistive Losses

Resistive losses happen when the light-generated carriers travel through the solar cell before being collected by the outside circuit. This loss mostly affects $FF$, which can be characterized by series-resistance ($R_s$) and shunt-resistance ($R_{sh}$) using equations (5)-(8) [5]. Major contributors of the $R_s$ are busbar resistance, gridline resistance, front contact resistance, emitter resistance, substrate resistance and back contact resistance, as illustrated in Figure 11. Ideality factor $n$ and $R_{sh}$ described the leakage current across the depletion region in-between the pn junction. Resistive losses are studied in detail in this thesis when designing the grid for the concentrator cells (Section 4.2) and selective emitter cells (Section 11.1).

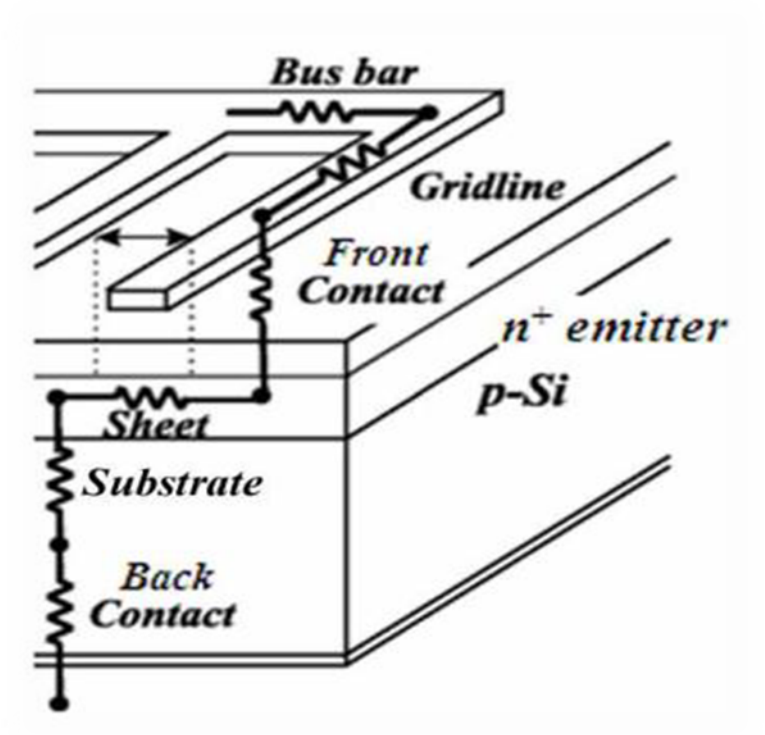



**Figure 11:** Series resistance components in a solar cell.

$$FF_o = \frac{v_{oc} - ln(v_{oc} + 0.72)}{v_{oc} + 1} \quad \text{for} \quad v_{oc} = \frac{qV_{oc}}{nkT} \tag{5}$$

$$R_{CH} = \frac{V_{oc}}{J_{sc}} \quad , \quad r_s = \frac{R_s}{R_{CH}} \quad \text{and} \quad r_{sh} = \frac{R_{sh}}{R_{CH}} \tag{6}$$

$$FF_s = FF_o(1 - r_s) \tag{7}$$

$$FF = FF_s \left[1 - \frac{(v_{oc} + 0.7)\, FF_s}{v_{oc} \cdot r_{sh}}\right] \tag{8}$$

### 2.2.6 Recombination

Recombination of carriers in the bulk, diffused regions, surfaces and metal can significantly reduce cell performance. The recombination is usually characterized by minority carrier lifetime, $\tau$, defined as

$$\tau \equiv \frac{\Delta n}{U} \tag{9}$$

where $\Delta n$ ($\mathrm{cm}^{-3}$) is the excess carrier concentration and $U$ ($\mathrm{cm}^{-3}/\mathrm{s}$) is the recombination rate. Following recombination mechanisms are discussed and studied in this research: (1) Auger Recombination, (2) Shockley-Read-Hall (SRH) recombination, (3) Surface Recombination, (4) Emitter/BSF Recombination.

#### *2.2.6.1 Auger Recombination*

Auger recombination involves three carriers and are dominant in heavily doped regions like emitter and BSF. The energy released from the electron-and-hole recombination is transferred to the third carrier (electron or hole) as shown in Figure 12. The total Auger recombination rate, $U_{Auger}$, is the sum of the two-electron process, $U_{eeh}$, and two-hole process, $U_{ehh}$, given by equation (10).

$$U_{Auger} = U_{eeh} + U_{ehh} = C_n n^2 p + C_p n p^2 \tag{10}$$

The Auger coefficients widely used are given by [19] as $C_n = 2.8 \times 10^{-31}$ $\mathrm{cm}^6/\mathrm{s}$ and $C_p = 9.9 \times 10^{-32}$ $\mathrm{cm}^6/\mathrm{s}$. Using equations (9) and (10), it can be shown that the Auger lifetime in n-type and p-type Si under low level injection (LLI) and high level injection (HLI) are given by equations (11)-(12):

$$\text{For n-type Si,} \quad \tau_{Auger,LLI} = \frac{1}{C_n {N_D}^2}, \quad \tau_{Auger,HLI} = \frac{1}{(C_n + C_p)\Delta n^2} \tag{11}$$

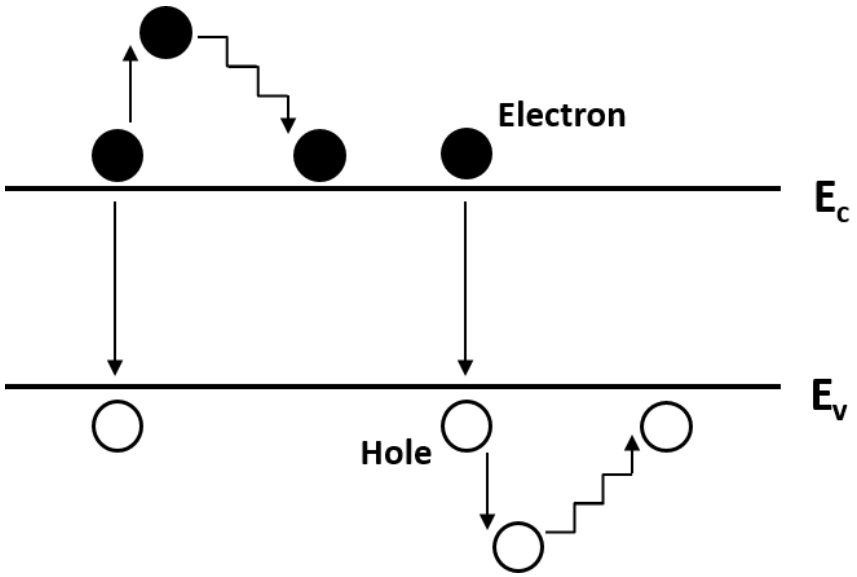



**Figure 12:** Energy band diagram for Auger recombination

$$\text{For p-type Si,} \quad \tau_{Auger,LLI} = \frac{1}{C_p {N_A}^2}, \quad \tau_{Auger,HLI} = \frac{1}{(C_n + C_p)\Delta n^2} \tag{12}$$

*2.2.6.2 Shockley-Read-Hall (SRH) Recombination*

SRH recombination occurs because of defect energy state within the bandgap, as shown in Figure 13. Normally, this is the dominant recombination process in the base of a Si solar cell under 1 sun illumination. The SRH recombination rate is given

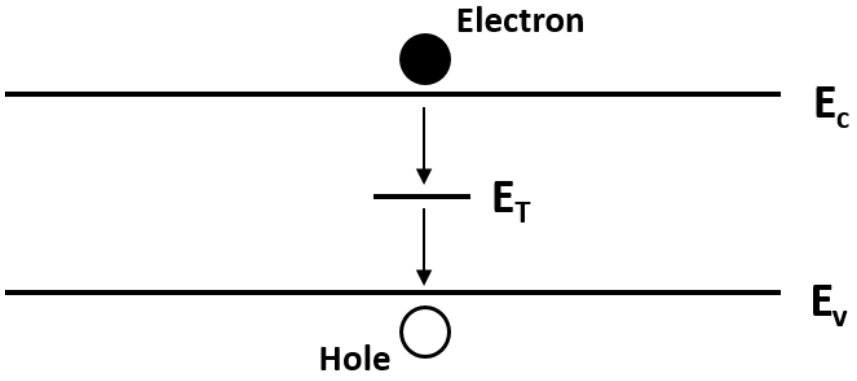



**Figure 13:** Energy band diagram for Shockley-Reda-Hall (SRH) recombination

by equation (13):

$$U_{SRH} = \frac{np - {n_i}^2}{\tau_{p0}(n + n_1) + \tau_{n0}(p + p_1)} \tag{13}$$

where $\tau_{p0}$ (s) and $\tau_{n0}$ are hole and electron lifetime, which are given by equation (14).

$$\tau_{p0} = \frac{1}{\sigma_p N_T v_{th}} \quad \text{and} \quad \tau_{n0} = \frac{1}{\sigma_n N_T v_{th}} \tag{14}$$

$\sigma_p$ ($\text{cm}^2$), $\sigma_n$, $N_T$ ($\text{cm}^{-3}$), and $v_{th}$ are hole capture cross section, electron capture cross section, trap density and electron thermal velocity ($\sim 10^7$ cm/s), respectively. $n_1$ and $p_1$ are given by equation (15), where $n_i$, $E_T$, $E_i$, $k$, and $T$ are intrinsic carrier concentration, trapping energy level, intrinsic energy level, Boltzmann constant and temperature, respectively.

$$n_1 = n_i exp\left(\frac{E_T - E_i}{kT}\right) \quad \text{and} \quad p_1 = n_i exp\left(\frac{E_i - E_T}{kT}\right) \tag{15}$$

Using equations (9) and (13), it can be shown that the SRH lifetime in n-type and p-type Si under low level injection (LLI) and high level injection (HLI)

$$\tau_{SRH,LLI} = \tau_{p0} + \frac{\tau_{p0} n_1 + \tau_{n0} p_1}{N_D}, \quad \tau_{SRH,HLI} = \tau_{n0} + \tau_{p0}, \text{ for n-type Si} \tag{16}$$

$$\tau_{SRH,LLI} = \tau_{n0} + \frac{\tau_{p0} n_1 + \tau_{n0} p_1}{N_A}, \quad \tau_{SRH,HLI} = \tau_{n0} + \tau_{p0}, \text{ for p-type Si} \tag{17}$$

If defects are at the midgap (deep trap), the LLI SRH lifetime can be simplified as:

$$\tau_{SRH,LLI} = \tau_{p0}, \text{ for n-type Si} \tag{18}$$

$$\tau_{SRH,LLI} = \tau_{n0}, \text{ for p-type Si} \tag{19}$$

*2.2.6.3 Surface Recombination*

There are large number of dangling Si bonds presenting at the Si surface, where electrons and holes can recombine (Figure 14). This recombination process is usually characterized by surface recombination velocity (SRV), $S$ (cm/s), which is defined by equation (20).

$$S \equiv \frac{U_s}{\Delta n} \tag{20}$$

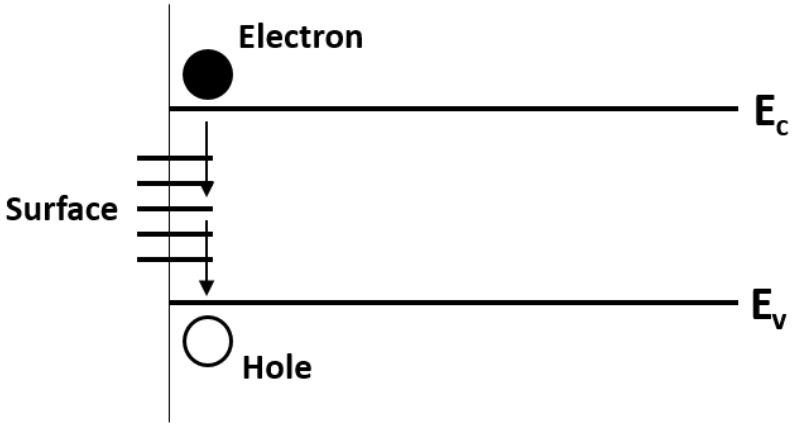



**Figure 14:** Energy band diagram for surface recombination

where $\Delta n$ ($\text{cm}^{-3}$) is the excess carrier concentration and $U_s$ ($\text{cm}^{-2}$/s) is the surface recombination rate. We can extend the SRH equation (13) to calculate the surface recombination rate from a single surface state.

$$U_S = \frac{S_{n0}S_{p0}(np - {n_i}^2)}{S_{n0}(n + n_1) + S_{p0}(p + p_1)} \tag{21}$$

where $S_{n0}$ (cm/s) and $S_{p0}$ are electron and hole surface recombination velocity given by equation (22).

$$S_{n0} = \sigma_n N_{ST} v_{th} \quad \text{and} \quad S_{p0} = \sigma_p N_{ST} v_{th} \tag{22}$$

$\sigma_n$ ($\text{cm}^2$), $\sigma_p$, $N_{ST}$ ($\text{cm}^{-2}$), and $v_{th}$ are electron capture cross section, hole capture cross section, surface trap density and electron thermal velocity (normally, $10^7$ cm/s), respectively. $n_1$ and $p_1$ are given by equation (15). Using equations (20) and (21), it can be shown that the SRV in n-type and p-type Si under low and high level injections can be expressed as

For n-type Si,

$$S_{LLI} = \frac{S_{p0}}{1 + \dfrac{K_D}{N_D}}, \text{ where } K_D = n_1 + \frac{S_{p0}}{S_{n0}} p_1 \tag{23}$$

$$S_{HLI} = \frac{S_{n0}S_{p0}}{S_{n0} + S_{p0}} \tag{24}$$

For p-type Si,

$$S_{LLI} = \frac{S_{n0}}{1 + \dfrac{K_A}{N_A}}, \text{ where } K_A = p_1 + \frac{S_{n0}}{S_{p0}} n_1 \tag{25}$$

$$S_{HLI} = \frac{S_{n0} S_{p0}}{S_{n0} + S_{p0}} \tag{26}$$

For defects at the midgap (deep trap), the LLI SRV can be simplified as

$$S_{LLI} = S_{p0}, \text{ for n-type Si.} \tag{27}$$

$$S_{LLI} = S_{n0}, \text{ for p-type Si.} \tag{28}$$

SRV can be decreased by minimizing the surface states, or by electrons and holes concentration at the surface. In practice, this is done by interface passivation (or chemical passivation) and field passivation. For interface passivation, a dielectric is deposited on top of Si surface in order to satisfy the dangling Si bonds to reduce $N_{ST}$. For field induced passivation, either electron or hole concentration at the surface is reduced by an electric field at the surface. Figure 15 (a) shows the band diagram for field induced passivation by applying a $p^+$ Back Surface Field (BSF) and Figure 15 (b) shows the field induced passivation by negative charge at the surface.

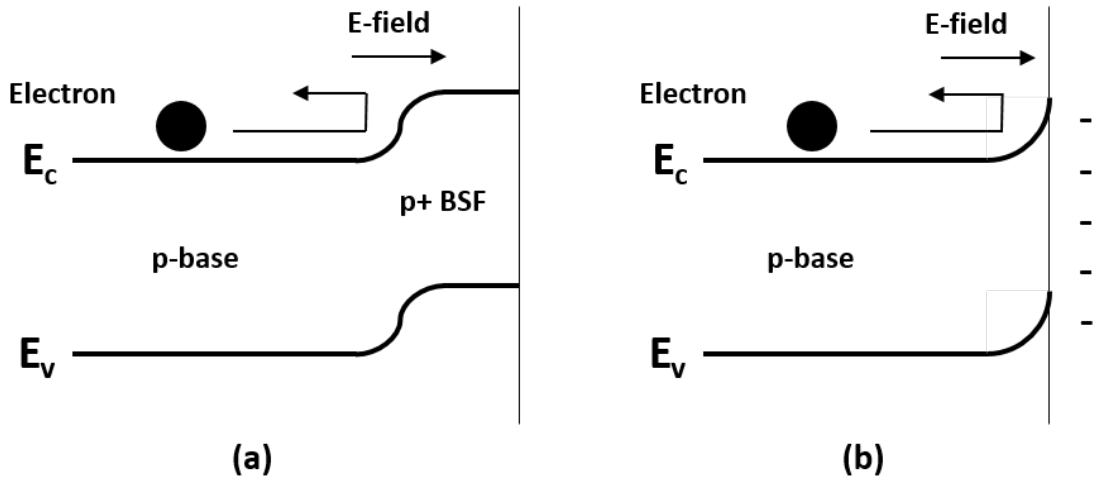



**Figure 15:** Energy band diagram for field passivation by (a) $p^+$ BSF and (b) negatively surface charge.

#### *2.2.6.4 Recombination in the Emitter, FSF and BSF Regions*

For simplicity, only emitter recombination is described in the section. However, the analysis is also true for all the heavily doped region in a solar cell such as FSF (front surface field) and BSF.

The recombination in the heavily doped emitter is relatively more complicated. Usually, we characterize such region by Effective Recombination Velocity ($S_{eff}$) or Emitter Saturation Current ($J_{0E}$), which includes the effects of surface recombination, Auger recombination and bandgap narrowing from the emitter, as shown in Figure 16. From [20], the minority emitter recombination current $J_{rec}$ is given by equation (29), where $D_{amp}$ is the ambipolar diffusion coefficient:

$$J_{rec} = J_{0E}\left(\frac{np}{{n_i}^2} - 1\right) = qU_s = q\Delta n S_{eff} = qD_{amp}\frac{d\Delta n}{dx} \tag{29}$$

For a p-base solar cell (Figure 16), $J_{0E}$ and $S_{eff}$ at the junction edge are related as follows:

$$S_{eff} = \frac{J_{0E}(N_A + \Delta n)}{q{n_i}^2} \tag{30}$$

$J_{0E}$ can be measured using the photo-conductivity decay method described in [20]. $\Delta n$ can be estimated from equation (31) with the applied voltage ($V_a$) across the junction.

$$V_a = \frac{kT}{q} ln\left[\frac{(n_0 + \Delta n)(p_0 + \Delta n)}{{n_i}^2}\right] \tag{31}$$

If we have the measured $J_{0E}$ number and emitter profile, SRV on the emitter surface (${S_p}^+$) can be calculated with the help of computer programs, such as PC1D and

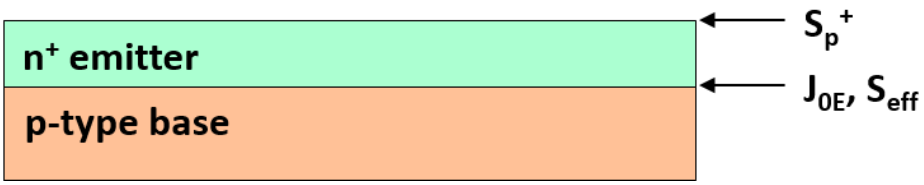



**Figure 16:** Schematic showing $J_{0E}$, $S_{eff}$, and ${S_p}^+$ in a p-type solar cell.

Sentaurus Device as explained later in Section 2.3.1. Experimentally, $S_p{}^+$ value has been found to be a function of surface concentration and dielectric technology ($SiO_2$, $SiN_x$, $AlO_2$, etc) [21, 22, 23, 24].

## *2.3 Understanding and Determination of Various Saturation Current Density Components in a Solar Cell*

Saturation current density of a region is indicative of total recombination in that region. One way to characterize the recombination in different regions in a solar cell is to develop a methodology to decompose the total saturation current density ($J_o$) into its components (Figure 17). Here, a p-type cell with highly doped n-type emitter on the front is used for illustration. The total $J_o$ is the sum of emitter saturation current density ($J_{oe}$) and base saturation current density ($J_{ob}$). As also shown in Figure 17, $J_{oe}$ can be sub-divided into the metal contribution $J_{oe.metal}$ and unmetallized passivated field contribution $J_{oe.field}$. $J_{ob}$ is sub-divided into the bulk contribution $J_{ob.bulk}$, the metal contribution $J'_{ob.metal}$, and unmetalliezed passivated field contribution $J'_{ob.field}$.

### 2.3.1 Determination of Front Metal and Passivated Field Contribution ($J_{oe.metal}$ and $J_{oe.field}$) to Emitter Saturation Current Density

If the emitter doping profile is known, we can use computer program to calculate $J_{oe}$ as function of $FSRV$ [25, 21, 26]. Note that this relationship would heavily depend on the physical models used for carrier statistics, carrier mobility, bandgap narrowing and Auger. In this thesis, both PC1D [27] and Sentaurus model were used. For Sentaurus, The physical models recommended by Pietro P. Altermatt [28] were selected, including Fermi-Dirac Statistics, Klaassens unified mobility model, Schenk bandgap narrowing model and Auger recombination coefficient from Dziewior and Schmid. A general definition of $J_{oe}$ was used (equation 32) and coded in Sentaurus

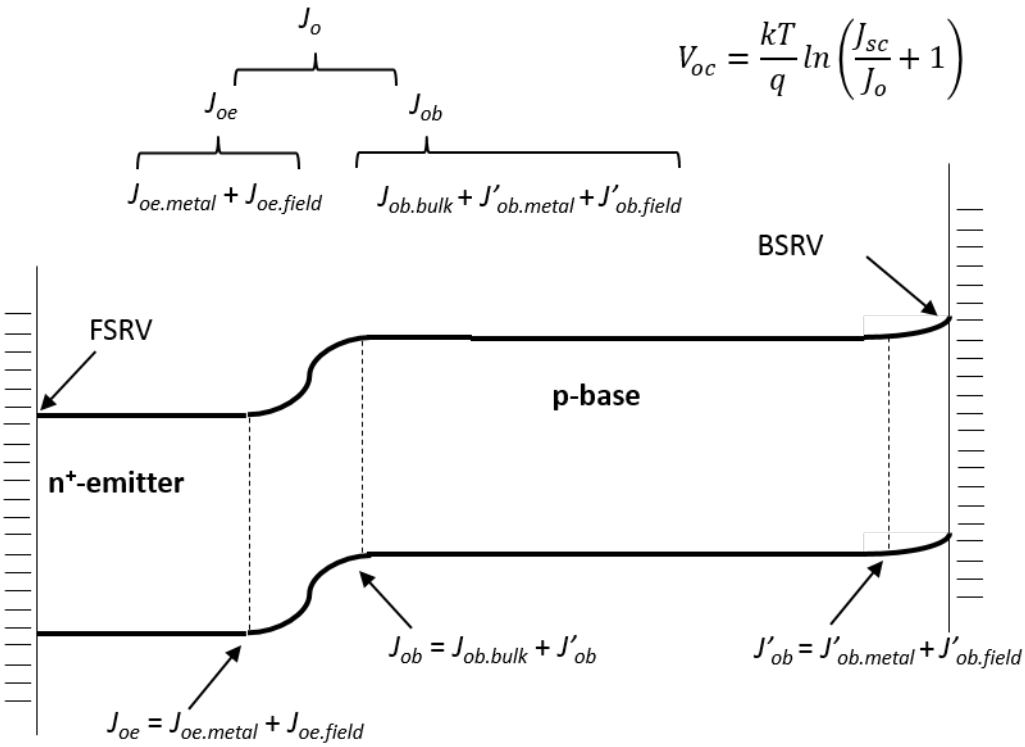



**Figure 17:** Band diagram of a $n^+p$ solar cell along with the illustration of its $J_o$ components.

model to extract the $J_{oe}$ in a $n^+p$ structure [25, 21, 26].

$$J_{oe} \equiv \frac{J_n(x_e)}{n(x_e)p(x_e) - n_i^2(x_e)} n_i^2(x_e) \tag{32}$$

where $x_e$ is the edge of the depletion region, and $J_n(x_e)$, $n(x_e)$, $p(x_e)$, and $n_i(x_e)$ are the electron recombination current, electron, hole and intrinsic carrier concentration at the junction $x_e$, respectively. For a given emitter profile, one can apply a fixed forward bias ($V_a$) in the model and obtain $J_n$, $n$, and $p$ values to calculate $J_{oe}$ vs $SRV$ curve using different $SRV$ values.

For example, Figure 18 shows a $n^+$ $POCl_3$ diffused emitter profile used in the thesis. Using this emitter profile and different $SRV$ values in Sentaurus model as input, we obtained $J_{oe}$ as function of $FSRV$ (Figure 19) for this profile (Figure 18). Now using the measured $J_{oe}$ of 74 fA/cm$^2$ for unmetallized passivated area ($J_{oe.field.full}$), $FSRV$ was extracted to be 7000 cm/s as shown in Figure 19. The $J_{oe}$

of 74 fA/cm$^2$ was measured on a symmetric test structure prepared with the same emitter and passivation dielectric on both sides. Full area $J_{oe.metal}$ ($J_{oe.metal.full}$) was calculated to be 1000 fA/cm$^2$ from Figure 19 since the $FSRV$ is $\sim 10^7$ cm/s under metal. Exact $J_{oe.metal}$ and $J_{oe.field}$ contribution is calculated using the area fractions of the metallized and unmetallized regions. For example, for a solar cell with 3.43% metal coverage and 96.57% unmetallized field region, $J_{oe.metal} = 3.43\% \times J_{oe.metal.full} = 3.43\% \times 1000$ fA/cm$^2$ = 34.3 fA/cm$^2$ and $J_{oe.field} = 96.57\% \times J_{oe.field.full} = 96.57\% \times 74$ fA/cm$^2$ = 71.5 fA/cm$^2$, resulting in a total $J_{oe}$ of 105.8 fA/cm$^2$.

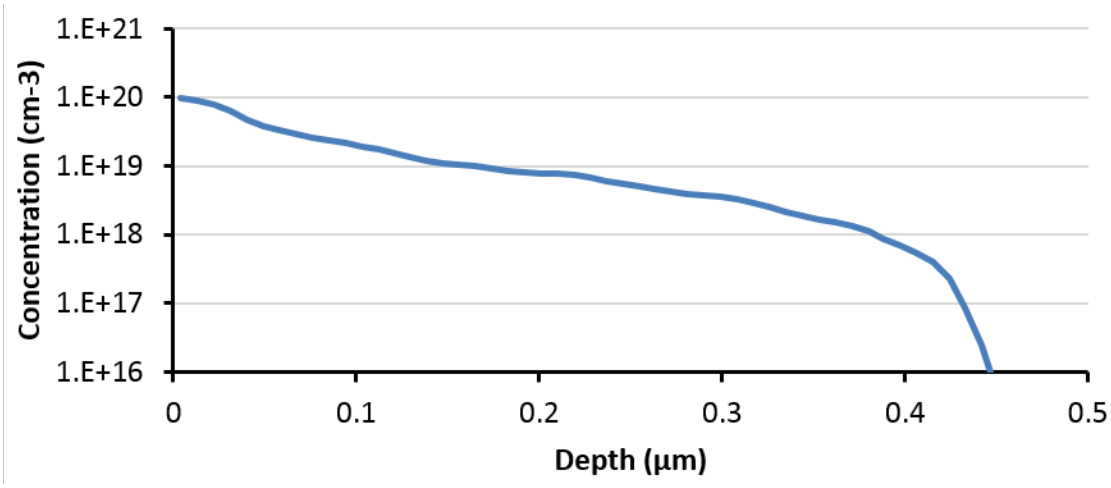



**Figure 18:** Measured phosphorus doping profile.

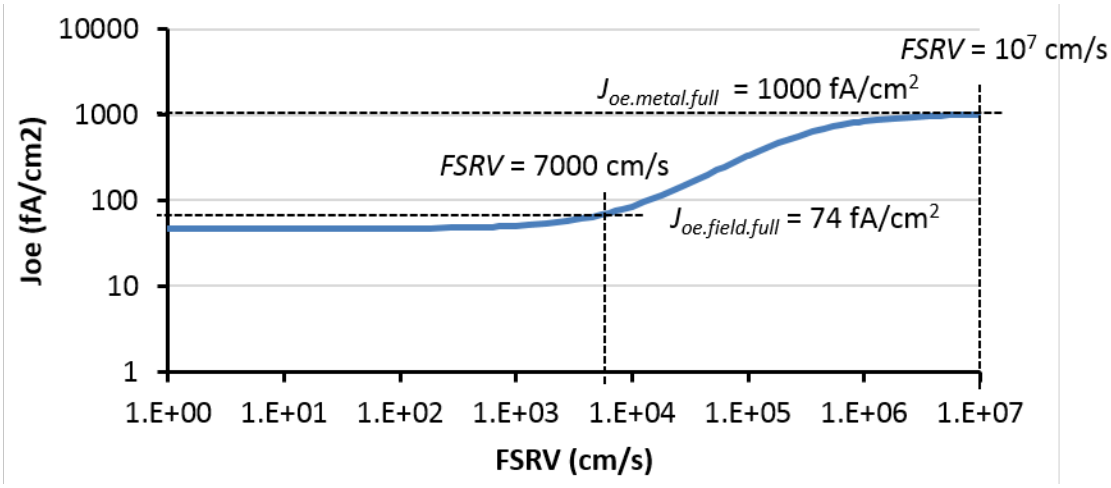



**Figure 19:** Modeled $J_{oe}$ vs $FSRV$ curve from Sentaurus model.

### 2.3.2 Determination of Bulk Recombination Contribution ($J_{ob.bulk}$) to Base Saturation Current Density

$J_{ob.bulk}$ is calculated using the following equation:

$$J_{ob.bulk} = qW\frac{n_i^2}{\tau_n N_A} \tag{33}$$

where $W$ is the wafer thickness and $\tau_n$ is the minority carrier lifetime. The equation (33) is derived from equation (34) for $S = 0$, $W \ll L_n$ and $tanh(W/L_n) \approx W/L_n$.

$$J_{ob} = \frac{qn_i^2}{N_A}\frac{D_n}{L_n}\frac{\frac{SL_n}{D_n} + tanh\frac{W}{L_n}}{1 + \frac{SL_n}{D_n}tanh\frac{W}{L_n}} \tag{34}$$

where $S$ is $BSRV$, $D_n$ is the minority carrier diffusion coefficient, and $L_n = \sqrt{D_n\tau_n}$. Note that this equation is derived for base under low level injection. For high level

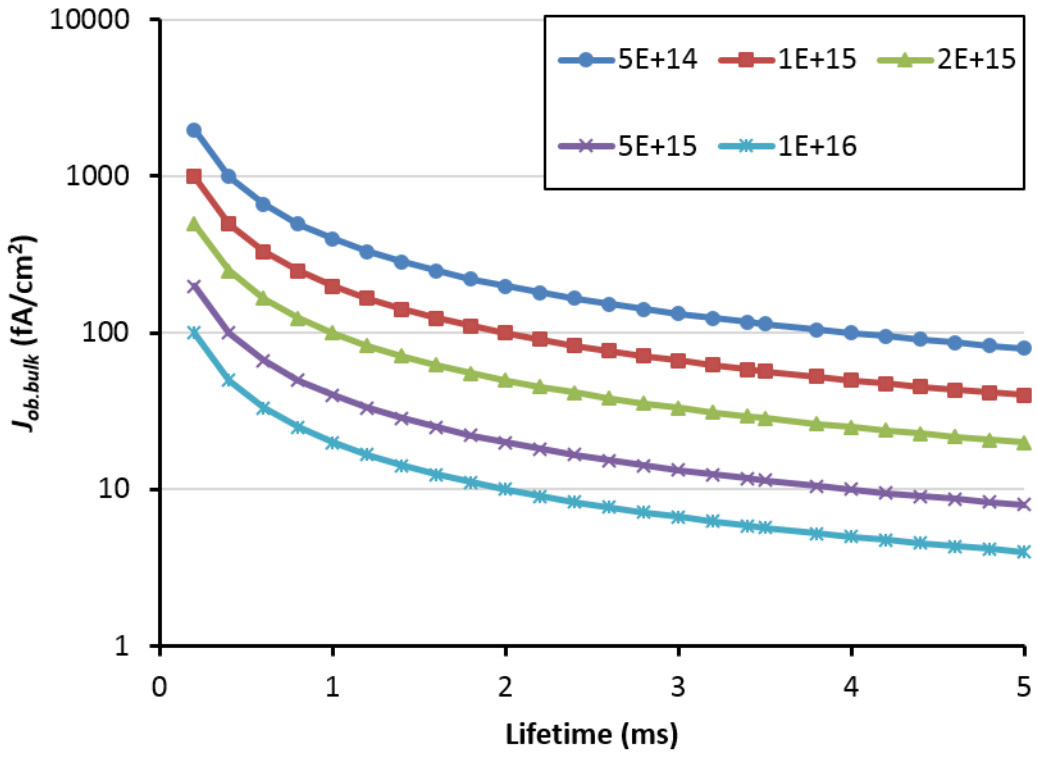



**Figure 20:** Calculated $J_{ob.bulk}$ as function of lifetime and $N_A$ for $W$=180 $\mu$m and $n_i = 8.3 \times 10^9$ cm$^{-3}$.

injection, one should use $J_{ob.bulk} \approx qW\frac{n_i^2}{\tau_{hli}(N_A+\Delta n)}$, where $\tau_{hli}$ is the minority carrier lifetime in high level injection. Figure 20 shows the calculated $J_{ob.bulk}$ as function of lifetime for $(N_A+\Delta n)$ in the range of $5\times10^{14}$ to $10^{16}$ cm$^{-3}$ with $W$=180 $\mu$m and $n_i = 8.3\times10^9$ cm$^{-3}$.

### 2.3.3 Determination of Back Metal and Passivated Field Contribution ($J'_{ob.metal}$ and $J'_{ob.field}$) to Base Saturation Current Density

Methodology used to calculate $J'_{ob.metal}$ and $J'_{ob.field}$ is very similar to $J_{oe.metal}$ and $J_{oe.field}$ in this thesis. $J'_{ob}$ is calculated using the following equation for a p$^+$n structure after obtaining $J_h$, $n$, and $p$ values at the junction after applying a fixed forward bias in the Sentaurus Device model.

$$J'_{ob} = \frac{J_h(x_e)}{n(x_e)p(x_e) - n_i^2(x_e)} n_i^2(x_e) \tag{35}$$

Note that the calculated $J'_{ob}$ for a p$^+$n structure should be very close to the p$^+$p structure. Experimentally, we have also observed that this $J_o$ number is independent of bulk wafer type and is governed by p$^+$ diffusion profile and passivation.

For a PERC solar cell, there is however no full area BSF on the back. We first measure $S_{eff}$ by symmetric test structure with dielectric passivation or matching long wavelength IQE of a cell and then $J'_{ob}$ is calculated by:

$$J'_{ob} = \frac{q{n_i}^2}{(N_A+\Delta n)} S_{eff} \tag{36}$$

Since this thesis involves many different promising cell designs and structures, above methodology to extract various $J_o$ components is used extensively to gain deeper insight into the pros and cons of various cell strategies.

## *2.4 Sentaurus 2D Modeling to Match a Solar Cell*

Sentaurus Device [29] is one of the most widely used multidimensional numerical CAD (computer aided design) programs for solar cell modeling. It is important for

a researcher to match a solar cell IV parameters with a device modeling program with experimentally measured inputs to gain better understanding of the device. By doing so, we can also develop roadmaps to guide the experiments by changing the model inputs and analyzing the outputs. This can drastically reduce the number of experiments. Many research groups have published solar cell modeling results to validate their findings and provide guidelines [30, 31, 32, 33]. Recently, Andreas Fell et al. published a review paper for the input parameters on the simulation of Si solar cells in 2014 [34].

In this thesis, solar cells with different structures were fabricated and matched using Sentaurus Device model and the experimentally measured inputs in Chapters VIII to X. To match a solar cell, we first need to build the unit cell resembling the experimental device. For a full back contact solar cell such as full Al-BSF, the width of the unit cell is half the spacing between the front fingers [28]. However, for a solar cell with local back contacts, wider unit cell is usually needed in order to have the front contacts symmetrically positioned with respect to the back contacts.

After the unit cell is built, the measured emitter profile, base resistivity, cell thickness, and BSF profile are used as inputs. We used the physical models recommended by Pietro P. Altermatt [28], which includes Fermi-Dirac Statistics, Klaassens unified mobility model, Schenk bandgap narrowing model and Auger recombination coefficient from Dziewior and Schmid. $FSRV$, minority lifetime, and $BSRV$ were varied or selected to match the measured $J_o$ in different regions as discussed in previous section (Section 2.3). Additional series resistance components including front contact, finger lines and busbars were added to the Sentaurus Device modeling, since the model only considers base and emitter sheet resistance components in the unit cell set up. All the series resistance components (contact resistance, sheet resistance, finger resistance, busbar resistance, bulk resistance and back contact resistance) can be extracted from test structures as discussed in more details in Chapter IV (Task I).

In this thesis, optical generation profiles from Sentaurus Device ray tracing program was used [29] with Phong reflection model [35] on the back surface. We found that the light generation profiles are not that critical in the final device modeling as long as the measured $J_{sc}$ is known and matched. By changing the light intensity, we can always match the measured $J_{sc}$ with different generation profiles. Similar $V_{oc}$ and $FF$ (less than 0.05% relative difference) for very different light generation profiles were obtained as long as the model output $J_{sc}$ is tuned to be the same by light intensity.

# CHAPTER III

# LITERATURE SURVEY

## *3.1 Screen-printed Low-medium Concentrator Si Solar Cell*

Concentrator solar cells carry much higher current than one sun cell. Therefore, their performance is very sensitive to series resistance and shading. Screen printing is the lowest cost, highest throughput, and most manufacturable contact technology for photovoltaic applications. However, screen-printed technology in the past was not suitable for concentrator Si solar cell because of wider line width ($\sim$150 $\mu$m), and higher series resistance compared to contact technologies like photolithography and plating [36]. Current increases linearly with the concentration ratio which increases $I^2R$ loss. Therefore, higher series resistance is much more detrimental for concentrator cells. That is why most screen-printed Si concentrator cells with a simple baseline cell design (full Al-BSF) in the past reported efficiencies below 17% [36, 37, 38] in the low to medium concentration range of 2-20 suns (X).

However, recent advances in Ag paste, screen material and design, and screen-printed technology have led to significant reduction in shadow and resistive losses which has created an opportunity for making low-cost high-efficiency low-medium concentrator solar cells. This is why Skyline Inc. is investigating 14X concentrator [39], Entech solar is developing 20X concentrator [40], JX crystal and Solaria are working on 3X concentrators [41, 42], and the Ohio State University is conducting research on 7X concentrator [43]. More recently, 19.8% efficient screen-printed cells at 3X were reported with advanced cell structures consisting of MWT-PERC contacts [44]. This provided the motivation in Task 1 (Chapter IV) to conduct research on this topic and achieve >20% efficient cells.

Since Si cells command ~90% of the PV market share today, manufacturing and availability of low-cost screen-printed low-medium concentrator Si solar cells should not be a problem if the 1X cell can be transformed into higher efficiency concentrator cell with little process modification. It is important to recognize that the primary difference between 1X cell and low-medium concentrator cell is simply the grid design: number of fingers and cell dimension [9]. Therefore, Task 1 (Chapter IV) focuses on design optimization and transformation of 1X commercial screen-printed Si solar cell into higher efficiency low-medium concentrator cells. This will be accomplished by a systematic approach of contact and device modeling to calculate the highest efficiency at a desired concentration from a given screen-printed paste, contact parameters, cell dimension, and printing technology followed by experimental validation and fabrication of high efficiency concentrator Si solar cells.

## *3.2 Thin Epi-Si Solar Cell on Low-Cost Substrate using Epitaxial Wafer Equivalent Structure*

Task 2-5 (Chapter VI-IX) in this thesis deals with a very promising and emerging Si wafer technology involving epitaxial growth of Si wafers which bypasses the use for Siemens reactor to grow feedstock Poly-Si, ingot growth, and wafer slicing. This not only reduces cost and energy for producing Si wafers but also eliminates the Kerf loss during slicing which could lead to >40% waste of Si in the form of Si dust. Epi-Si wafers can be grown directly on a Si substrate by CVD of $SiHCl_3$ gas. This

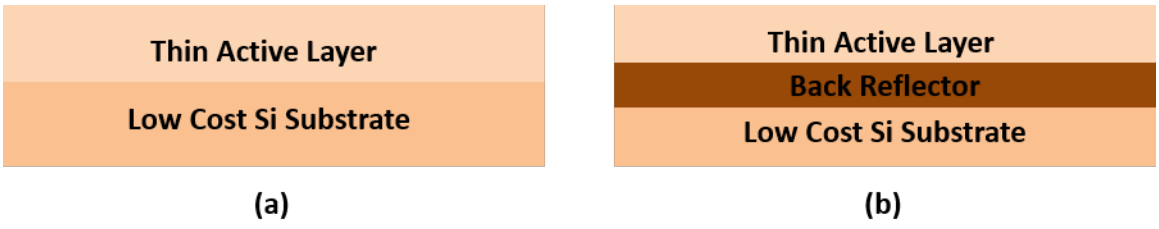



**Figure 21:** The cross-section schematic of Epitaxial Wafer Equivalent (EpiWE). (a) EpiWE without back reflector. (b) EpiWE with back reflector

**Table 1:** Literature survey of epitaxial wafer equivalent Si solar cells

| Year | [1]Epi-W ($\mu$m) | Eff (%) | $V_{oc}$ (mV) | $J_{sc}$ (mA/cm$^2$) | FF (%) | Area (cm$^2$) | Institute | Front Con. | [2]PSI BR. | Technology Highlight | Ref. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1994 | 50 | 17.3 | 655 | 32.5 | 81.7 | 4 | MPI-FKF | [3]PL | | Diffused selective emitter, inverted pyramid tex. | [47, 48] |
| 1996 | 32 | 16.4 | 645 | 32.3 | 78.5 | 4 | UNSW | PL | | Liquid phase epitaxy, V-microgrooves tex. | [49] |
| 1996 | 32 | 17.6 | 661 | 32.8 | 82.2 | 4 | UNSW | PL | | n-p-n-p-n-p+ structure, inverted pyramid tex. | [50] |
| 1998 | 37 | 17.6 | 661 | 32.5 | 82.2 | 4 | FhG ISE | PL | | Diffused selective emitter, inverted pyramid tex. | [51] |
| 2004 | 35 | 15.2 | 649 | 29.4 | 79.7 | 143 | FhG ISE | PL | | Large area, random pyramid tex. | [52] |
| 2004 | 35 | 11.6 | 617 | 25.7 | 73.2 | 96 | FhG ISE | [4]SP | | Large area, random pyramid tex. | [52] |
| 2005 | 20 | 12.8 | 618 | 26.9 | 76.6 | 98 | IMEC | SP | | Large area, plasma tex. | [53] |
| 2008 | 18 | 14.9 | 655 | 28.4 | 79.9 | 92 | FhG ISE | PL | | Epitaxially grown emitter | [54] |
| 2008 | 21 | 15.2 | 648 | 29.6 | 79.5 | 4 | FhG ISE | PL | | Epitaxially grown emitter, plasma tex. | [55] |
| 2009 | 25 | 16.9 | 627 | 34.6 | 78 | 4 | IMEC | PL | ✓ | n-type, 2-step emitter, random pyramid tex. | [56] |
| 2009 | 20 | 14.2 | 605 | 31.2 | 75 | 71 | IMEC | SP | ✓ | Large area, plasma tex. | [57] |
| 2010 | 20 | 16.1 | 621 | 33.2 | 78 | 4 | IMEC | PL | ✓ | 2-step emitter, plasma tex. | [58] |
| 2010 | 19 | 15.2 | 627 | 31.3 | 77.2 | 73 | IMEC | PL | ✓ | Large area, plasma tex. | [45] |
| 2011 | 50 | 16.5 | 645 | 32.7 | 78.3 | 4 | FhG ISE | PL | | Basic and simple cell process | [59] |
| 2012 | 30 | 16.2 | 634 | 31.7 | 80.8 | 70 | IMEC | PL | ✓ | Large area, n-type, random pyramid tex. | [46] |
| 2013 | 28 | 14.1 | 630 | 28.5 | 78.7 | 4 | FhG ISE | PL | | Epitaxially grown emitter, overgrown $SiO_2$ | [60] |

Note that the cell processes and structures can be significantly different from one another as noted in Technology Highlight.[1]Epi-W: Epi-Si thickness. [2]PSI BR.: porous silicon back reflector. [3]PL:photolithography defined contact. [4]SP: screen-printed contact

provides a huge opportunity for cost reduction because Si wafer is the most expensive component (30-33%) in a PV module [3]. Epi-Si wafers can be grown and used in several different configuration for PV application. One promising way is to use the Epitaxial Wafer Equivalent (EpiWE) structure (Figure 21 (a)), which involves an epitaxially grown Si active layer on top of a highly doped Si substrate [45, 46]. The Si material cost is reduced because the cost of epi-grown high quality active thin layer ($<100\mu$m) on top of the inactive low-cost and low-quality Si substrate is cheaper than using a high quality thick wafer [45, 46]. In order to attain high efficiency from thin epitaxially grown active layer, generally, a back reflector (thin porous Si layer) is required between the epi-Si layer and the substrate, as shown in Figure 21 (b).

The EpiWE concept has been investigated for about 20 years as shown in Table 1. Efficiencies in the range of 11.6$\sim$17.6% have been reported with epi-Si layer thickness

in the range of 20∼50 $\mu$m. Porous Si (PSI) back reflector was first introduced by J. Zettner et al. for thin Si solar cell [61] followed by several papers on EpiWE cells with PSI back reflector [56, 57, 58, 45, 46] (Table 1). However, very few screen-printed large-area cells have been attempted using the EpiWE structure. In fact, there are even fewer EpiWE cells made with both screen-printed contact and PSI back reflector. The one we could find in the literature [57] had an efficiency of 14.2% on 20 $\mu$m thick epitaxially grown Si with an area of 71 cm$^2$. This provided the motivation in Task 2 (Chapter VI) to fabricate high efficiency large-area screen-printed epi-Si cells on low-cost substrate using EpiWE structure with the porous Si layer.

## *3.3 Thin Epi-Si Solar Cell without Substrate using Porous Si Layer Transfer Process*

Epi-Si growth on reusable Si substrate with porous Si layer in between provides a unique opportunity to exfoliate the epi-Si layer by mechanical force. This allows one to lift off the thin epi-Si cell and reuse the substrate for next epi-Si wafer.

Laboratory cell efficiency of 21.5% on 47±1 $\mu$m Si wafers (etched from a regular thickness Si wafers) was reported using the PERL cell structure in 1996 [62], which required many photo masking and high temperature steps. Therefore, it was not a manufacturable process but provided a proof of concept that high efficiency Si solar cells can be achieved on <50 $\mu$m thick Si. The layer transfer process with porous silicon (PSI) was introduced by Tayanaka and Matsushita [63] and Brendel [64] to solve the problem of processing thin Si. The sketch of the fabrication schemes is shown in Figure 22 [65]. The PSI layer provides a good seed layer for ep-Si growth and permits the transfer of the device layer from a reusable substrate to a carrier at the same time [65]. Kerf loss is therefore greatly reduced by the reuse of the same substrate. In fact, T.S. Ravi et al. demonstrated 50 times substrate reuse with no degradation in the quality or bulk lifetime of the epi-Si wafers as well as the physical quality of the substrate [6].

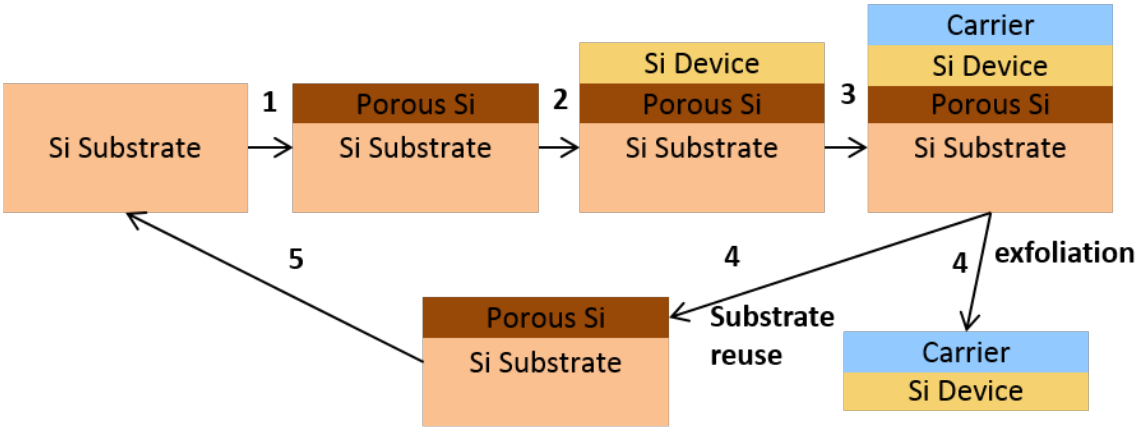



**Figure 22:** The sketch of layer transfer process with PSI. (Step 1) PSI formation. (Step 2) Si device layer formation. (Step 3) Carrier attachment. (Step 4) Separation of Si device and substrate. (Step 5) Cleaning and resuse of substrate [65].

**Table 2:** Literature survey of epi-Si solar cells using layer transfer with PSI

| Year | [1]Epi-W ($\mu$m) | Eff (%) | $V_{oc}$ (mV) | $J_{sc}$ (mA/cm$^2$) | FF (%) | Area (cm$^2$) | Institute | Front Con. | Back Con. | Carrier | Technology Highlight | Ref. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1998 | 12 | 12.5 | 623 | 25.5 | 79.0 | 4 | Sony Inc. | N/A (Al) | Full [2]p-Ag | Plastic | Diffused selective emitter | [63] |
| 2001 | 15.5 | 12.2 | 600 | 25.6 | 79.2 | 2.1 | ZAE Bayern | [3]SME | Full [4]e-Al | Glass | [5]RP tex. | [66] |
| 2001 | 20 | 9.5 | 520 | 27.5 | 66.3 | 0.2 | Canon Corp. | N/A | Full Al | Si | Liquid phase-epitaxy | [67] |
| 2002 | 46.5 | 16.6 | 645 | 32.8 | 78.2 | 4 | IPE Stuttgart | [6]PL | Full e-Al | Glass | RP tex. | [68] |
| 2003 | 26 | 15.4 | 623 | 32.7 | 75.5 | 3.88 | ZAE Bayern | SME | SME Al Grid | Glass | RP tex. | [69] |
| 2007 | 24 | 14.5 | 588 | 33.3 | 74.2 | 4 | ISFH | SME | SME Al/Ag Grid | Glass | Autodiffused emitter, RP tex. | [70] |
| 2009 | 47 | 17.0 | 634 | 36.0 | 74.6 | 1.1 | IPE Stuttgart | PL | Full e-Al | Free | RP tex. | [71] |
| 2009 | 41.6 | 16.9 | 641 | 33.5 | 78.7 | 2 | IPE Stuttgart | PL | [7]LFC | Glass | RP tex., a-Si:H/SiN$_x$ back pass. | [71] |
| 2011 | 43 | 19.1 | 650 | 37.8 | 77.6 | 4.0 | ISFH | SME | [8]LOC | Free | RP tex., $Al_2O_3$ pass. | [72] |
| 2012 | 43 | 20.1 | 682 | 38.1 | 77.4 | 243 | Solexel Inc. | N/A | N/A | Plastic | Back interdigital contact | [73] |
| 2013 | 20 | 14.4 | [9]- | [9]- | [9]- | 54 | UNSW | Ni/Cu plating | Point contact | Steel | Laser doped Selective [10]FSF | [74] |
| 2014 | 18 | 16.8 | 632 | 34.5 | 77.2 | 4 | UNSW | Ni/Cu plating | Point contact | Steel | Laser doped Selective FSF | [75] |
| 2014 | 21.6 | 13.6 | 613 | 31.5 | 70.4 | 81 | ISFH | SME | LOC | Poly-Si | RP tex., $Al_2O_3$ front pass. | [76] |

Note that the cell processes and structures can be significantly different from one another as noted in Technology Highlight.[1]Epi-W: Epi-Si thickness. [2]p-Ag: paste Ag. [3]SME: shadow mask evaporation. [4]e-Al: evaporated Al.[5]RP tex. random pyramid texture. [6]PL: photolithography. [7]LFC: laser fired point contact. [8]LOC: laser opening point contact [9]N/A in the published paper. [10]FSF: front surface field.

Epi-Si cells made by various investigators in the last 16 years by the PSI layer transfer process are summarized in Table 2. The efficiency has improved dramatically

from 12.5% (4 $cm^2$, 12 $\mu$m Si) to 20.1% (243 $cm^2$, 43 $\mu$m Si). Although some small area free-standing thin Si cells have been demonstrated, large area cells were made by using different carrier, such as plastic, steel and Poly-Si. As shown in Table 2, different metal contact technologies were chosen by different groups. However, no one reported on the use of screen-printed contacts to large area low-cost front junction epi-Si cells using PSI layer transfer process. This provided the motivation to fabricate high efficiency screen-printed front junction thin epi-Si solar cells using PSI layer transfer process in Task 3 (Chapter VII) in the thesis.

## *3.4 Free-standing Thick Epi-Si Kerfless Wafer*

Although cells made from thin (40-90 $\mu$m) epi-Si show good efficiency and great potential for cutting down the solar module price, they are too thin to be processed or packaged directly with high yield using current cell and module technology. The average wafer thickness for Si cells in industry today is $\sim$180 $\mu$m because of the yield decreases with thin cells but is expected to go down to 150 $\mu$m and 120 $\mu$m by 2019 and 2025, respectively, as predicted by 2015 International Technology Roadmap for Photovoltaic [3]. If wafers with thickness of 120-150 $\mu$m can be processed with high yield into a module, then epi-Si wafers using the PSI layer transfer process can be much more cost effective than the traditional ingot/slicing technology.

In the past, somewhat lower bulk lifetime in epi-Si layers was a concern for thicker stand alone epi-Si cells. Therefore, many groups around the globe have been investigating the minority carrier lifetime issue in the epi-Si produced by PSI layer transfer process, including Fraunhofer ISE [77] and IMEC [78]. Recently, Crystal Solar Inc., our collabarator in this research, reported 780 $\mu$s and 2 ms effective lifetime in a 2 $\Omega$-cm p-type and 2 $\Omega$-cm n-type epi-Si material by intentional gettering treatment, respectively [6]. These lifetime numbers are good enough for 120-180 $\mu$m thick wafers to produce high efficiency cells. In addition, throughput of >300 wafers/hour can be

obtained for these thick free-standing epi-Si wafers by a multiple chambers hardware design and the wafer cost can be 50% lower compared to standard Cz wafers [6]. This provided the motivation in Task 4 (Chapter VIII) to demonstrate ≥20% large area screen-printed Si solar cell on ≥120 $\mu$m thick p-type and n-type epi-Si wafers using PSI layer transfer process.

## *3.5 Epi-Si Solar Cell with Built-in Junctions*

Since the doping level in epi-Si can be easily controlled by adding the dopant gas to the silicon precursor, it is possible to grow in-situ the base as well as doped regions, such as FSF (front surface field), emitter, and BSF (back surface field ), in a simple epi run. The in-situ epitaxially grown emitter or BSF on top of the epi-grwon base provides several advantages. First, it simplifies the process sequence because there is no need for extra diffusion steps to from the emitter. Second, it increases throughput because the epitaxy of emitter takes less than 10 minutes (growth rate ∼4 $\mu$m/min) while the emitter diffusion usually takes couple of hours (including temperature ramping up and down). Third, the doping profile of epitaxial emitter can be controlled to realize a deep and lightly doped emitter to minimize Auger recombination and achieve surface passivation. For example, a $10^{17}$ cm$^{-3}$ doped 20 $\mu$m deep emitter with an abrupt profile can provide low sheet resistance in the range of 40-100 Ω/sq. The Auger-limited diffusion length is around 500 $\mu$m (920 $\mu$m) in this $10^{17}$ cm$^{-3}$ n-type (p-type) Si, which is sufficient for minority carrier to travel through the 20 $\mu$m thick [1]emitter region. The surface passivation for this emitter is also expected to be much better because of the low surface doping concentration compared to traditionally diffused emitter [21, 22], which usually has $10^{19}$-$10^{20}$ cm$^{-3}$ doping and surface concentration. However, $10^{17}$ cm$^{-3}$ emitter surface concentration will require selective emitter to make good ohmic contact. Fourth, no phosphorus or boron silicate glass are formed

[1]The sheet resistance and diffusion length numbers are from PC1D model [27].

on top of the epitaxially grown emitter, which eliminates the extra steps of removing the diffusion glass, chemical cleaning, and etching.

**Table 3:** Literature survey of epi-Si solar cells with in-situ emitter

| Year | [1]Epi-W ($\mu$m) | Eff (%) | $V_{oc}$ (mV) | $J_{sc}$ (mA/cm$^2$) | FF (%) | Area (cm$^2$) | Institute | Front Con. | Cell struc. | Process | Ref. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1996 | 32 | 17.6 | 661 | 32.8 | 82.2 | 4 | UNSW | [2]PL | Multi EpiWE | In-situ p$^+$n-p-n-p-n⇒ tex.⇒ phos diffusion⇒ [3]pass., metal, [4]ARC | [50] |
| 2008 | 18 | 14.9 | 655 | 28.4 | 79.9 | 92 | FhG ISE | PL | [5]FJ-p, EpiWE | In-situ pn$^+$ ⇒ pass., metal, ARC | [54] |
| 2008 | 21 | 15.2 | 651 | 28.9 | 80.6 | 4 | FhG ISE | PL | FJ-p, EpiWE | In-situ pn$^+$ ⇒tex.⇒ $POCl_3$ FSF⇒ pass., metal, ARC | [55] |
| 2009$^{(a)}$ | 20 | 16.1 | 621 | 33.2 | 78 | 4 | IMEC | PL | FJ-p, EpiWE | In-situ p$^+$pn⇒ tex.⇒ epi [6]FSF⇒ pass., metal, ARC | [56] |
| 2009$^{(b)}$ | 20 | 15.5 | 635 | 31.5 | 77 | 4 | IMEC | PL | FJ-p, EpiWE | In-situ p$^+$p, tex.⇒ epi nn$^+$ emitter FSF⇒ pass., metal, ARC | [56] |
| 2009$^{(c)}$ | 25 | 16.9 | 627 | 34.6 | 78 | 4 | IMEC | PL | [7]BJ-n, EpiWE | In-situ p$^+$n, tex.⇒ $POCl_3$ FSF⇒ pass., metal, ARC | [56] |
| 2014 | 18 | 16.8 | 632 | 34.5 | 77.2 | 4 | UNSW | Ni/Cu plating | BJ-n, [8]LT | In-situ n$^+$np$^+$, ⇒ pass., point contact, layer transfer to steel⇒ tex., PECVD, laser doped selective FSF, metal | [74] [75] |

Note that the cell processes and structures can be significantly different from one another as noted in Technology Highlight.[1]Epi-W: Epi-Si thickness. [2]PL: photolithography. [3]pass.:surface passivation. [4]ARC: Anti-reflection coating.[5]FJ-p: p-base front junction solar cell. [6]FSF: front surface field. [7]BJ-n: n-base back junction solar cell. [8]LT: layer transfer process by PSI.

The concept of growing emitter epitaxially is widely used in III-V solar cells and Si hetero-junction solar cell [54]. Table 3 summarizes the literature on epi-Si solar cells with in-situ epitaxial emitter. In 1996, G. F. Zheng et al. reported a 17.6% efficient multilayer epi-Si cell [50], with p-type and n-type layers and five PN-junctions with a doping of $10^{17}$ cm$^{-3}$. Texturing process (microgrooved and inverted pyramid) was controlled very precisely as the stack of epi-Si was finished before texturing. E. Schmich et al. showed 14.9% large area (92 cm$^2$) epi-Si cell with in-situ epi-grown emitter on planar surface in 2008 [54]. They concluded that very little recombination takes place in the epi-Si PN-junction space charge region as indicated by very low measured dark current $I_{02}$. Next, 15.2% efficient epi-Si cell with in-situ emitter on textured surface was reported by E. Schmich et al. [55]. The plasma texturing was performed after the growth of 1 $\mu$m thick epi-Si emitter. Some cells showed shunting

because of the un-optimized (too much) texturing. An extra $POCl_3$ diffusion was done after texturing to get the shunt resistance back to normal. In 2009, K. V. Nieuwenhuysen et al. compared 3 different epi-Si cell processes with in-situ emitter [56]: (a) Front junction p-type cell with in-situ emitter before texturing followed by an FSF implemented by a second epitaxial growth. (b) Front junction p-type cell with epi-Si emitter and FSF after texturing. (c) Back junction n-type cell with $POCl_3$ FSF after texturing. These results showed that the back junction n-type cell with in-situ p-type emitter gave the highest efficiency of 16.9%. Recently, 16.8%, 18 $\mu$m thick back junction epi-Si cell using layer transfer process was demonstrated by A. Lochtefeld and L. Wang, in UNSW [74, 75]. Back contact was made by point Al contact and a selective FSF was formed by laser $n^+$ doping and Ni/Cu plated contact. This provided the motivation in Task 5 (Chapter IX) to model and develop high efficiency large area screen-printed epi-Si solar cells with in-situ BSF ($pp^+$) and emitter ($n^+pp^+$).

## *3.6 Tunnel Oxide Passivated Contact Solar Cell*

Carrier selective passivating contacts provide the opportunity to decouple or physically displace the doped and metallized regions outside the absorber. This could lead to much higher $V_{oc}$ because it is not limited by the fermi levels of the doped regions, instead it is dictated by the quasi fermi level split dictated by the bulk lifetime and injection level in the absorber. The best example of this is the HIT solar cell structure where a very thin (10 nm) intrinsic a-Si:H layer is used to physically displace the doped a-Si:H regions and metal contacts outside the absorber while providing excellent passivation to the Si surface. Reduced recombination in the doped and metallized regions is achieved by carrier selectivity offered by band offsets, which favors the flow of only one type of carriers on each side of the absorber. Carriers can easily tunnel or hop through the i-layer into the doped regions which transport them

to the metal. That is why HIT technology has recently produced 750 mV $V_{oc}$ [79] and 25.6% efficiency [80]. Other examples of carrier selective contacts include tunnel oxide layer between the absorber and a-Si:H regions [81, 82], and the use of $MoO_x$ [83] and $TiO_2$ [84] for the hole and electron selective contacts, respectively. However, all the above passivated contact technologies are not compatible with the industry standard low-cost screen-printing and firing process since they cannot withstand high temperature. The Semi-Insulating Polycrystalline Silicon (SIPOS) is another carrier selective contacts which can withstand high temperature process and has achieved $V_{oc}$ of 720 mV [85]. Fraunhofer ISE recently introduced a tunnel oxide passivated contact (TOPCon) [12], in which a $\sim$1.5 nm thick tunnel oxide is used to displace doped Poly-Si and metal regions outside the absorber. They have demonstrated small area (4 $cm^2$) 24.9% efficient cells on Fz silicon with photolithography (PL) contacts, boron doped selective emitter on the front, and a full area TOPCon back contact composed of tunnel oxide capped with deposited full area $n^+$-doped Poly-Si layer and metal [13]. However, no one had demonstrated a TOPCon cell with screen-printed contacts using manufacturable technologies and commercial grad Cz Si. This provided the motivation in Task 6 (Chapter X) to develop a methodology to model TOPCon based cells, validate it by matching the Fraunhofer 24.9% TOPCon cell, and extending the model to estimate the efficiency potential of screen-printed TOPCon cells on Cz Si.

# CHAPTER IV

# TASK 1: DEVELOPMENT OF HIGH EFFICIENCY SCREEN-PRINTED LOW-MEDIUM CONCENTRATOR SI SOLAR CELLS

This chapter deals with device modeling and a methodology to achieve low-cost high-efficiency screen-printed low to medium concentrator Si solar cells. The model is then validated by fabricating some of the most efficient metal paste printed cells using the most simple full Al-BSF Si cell structure. The model also shows that the Highest Achievable Efficiency (HAE) at any given concentration is a function of metal paste, contact parameters, and grid pattern due to the trade-off between resistive and shadow losses. Consistent with the model calculations, first 52×78 mm screen-printed cells were fabricated using ∼110 $\mu$m wide finger and 1.37 mm spacing with Dupont 16A paste. These cells gave an efficiency of 18.9% at 4 suns (X). The cell efficiency was then improved to 19.0% at 4-5X with 1.63 mm finger spacing and shorter finger (25 mm of effective finger length). Finally, 50 $\mu$m wide direct extrusion printed fingers were applied, which resulted in >20% efficient cells in the concentration range of 3-16X, along with a roadmap to achieve ≥21% efficient cells. The methodology developed and used in this research provides excellent guidelines for designing grid patterns to achieve maximum efficiency at the desired concentration from a given front paste printing technology and one sun cell structure.

## *4.1 Development of an Analytical Model to Calculate Cell Efficiency under Various Concentrations*

First step in this methodology involves calculating the efficiency as a function of concentration. Model starts with equation (37) to calculate $J_o$ from $J_{sc}$ and $V_{oc}$ values at one sun (1X). As a first order approximation, $J_{sc}$ was assumed to increase linearly with concentration [86] and calculated at different concentrations ($J'_{sc}$) according to equation (38). $V'_{oc}$, $FF'$ and cell efficiency at different concentrations or suns were calculated using equations (39) to (44) [5]. The above model was validated by designing a grid pattern and fabricating few test concentrator cells. These concentrator cells have one-sun measured values of $J_{sc} = 35.3$ mA/cm$^2$, $V_{oc} = 618$ mV, $R_s = 0.164$ Ω-cm$^2$, $R_{sh} = 893$ Ω-cm$^2$ and ideality factor $n \approx 1$ in average. Using these measured

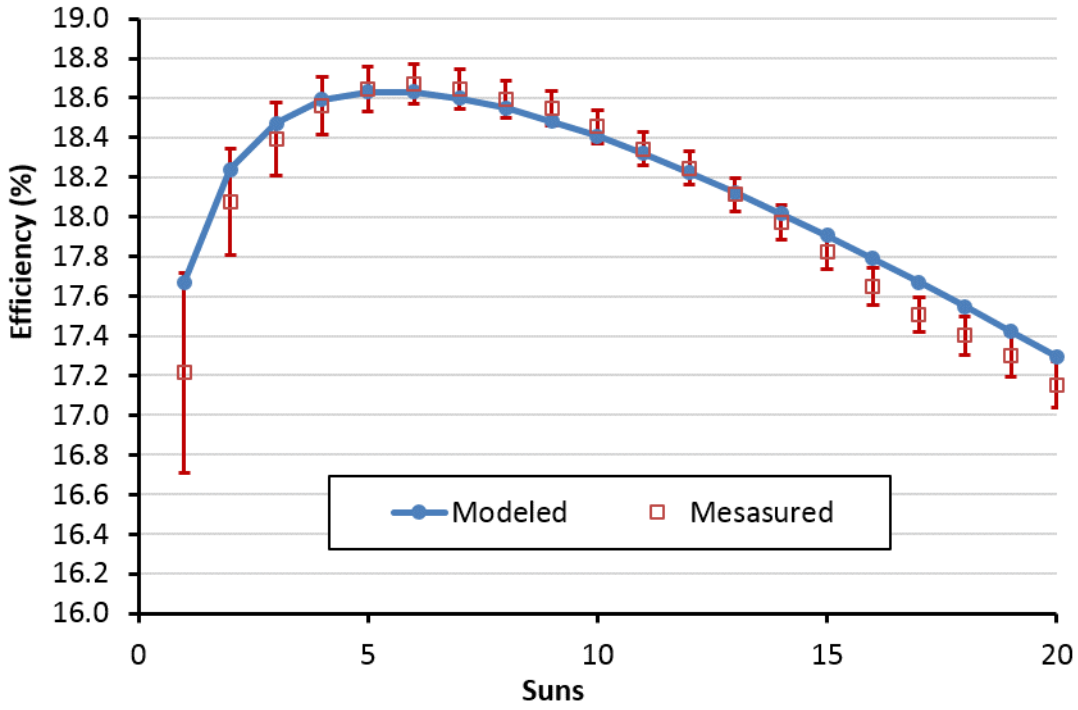



**Figure 23:** Comparison of modeled and measured efficiency versus suns curve to validate the analytical model.

one-sun values and equations (37) to (44), we calculate efficiency as a function of concentrations as shown in Figure 23, which shows a good match between the modeled and measured efficiency in the concentration range of 1-20X. Note that the efficiency and $J_{sc}$ were measured and calculated with aperture area without busbars [87]. All the concentrator-cell efficiency numbers reported in this task are using aperture area.

$$J_o = J_{sc}(e^{qV_{oc}/kT} - 1)^{-1} \tag{37}$$

$$J'_{sc} = x \cdot J_{sc} \tag{38}$$

$$V'_{oc} = \frac{kT}{q} ln\left(\frac{J'_{sc}}{J_o} + 1\right) \tag{39}$$

$$FF_o = \frac{v_{oc} - ln(v_{oc} + 0.72)}{v_{oc} + 1} \quad \text{for} \quad v_{oc} = \frac{qV'_{oc}}{nkT} \tag{40}$$

$$R_{CH} = \frac{V'_{oc}}{J'_{sc}} \quad , \quad r_s = \frac{R_s}{R_{CH}} \quad \text{and} \quad r_{sh} = \frac{R_{sh}}{R_{CH}} \tag{41}$$

$$FF_s = FF_o(1 - r_s) \tag{42}$$

$$FF' = FF_s\left[1 - \frac{(v_{oc} + 0.7)\, FF_s}{v_{oc} \cdot r_{sh}}\right] \tag{43}$$

$$\eta = \frac{V'_{oc} \cdot J'_{sc} \cdot FF'}{P_{in}} \tag{44}$$

## *4.2 Determination of One-sun $V_{oc}$, $J_{sc}$, $R_s$, $R_{sh}$ and n-factor for Different Finger Spacings*

Grid design is the key to making high efficiency concentrator cell from a one-sun cell structure and achieving the maximum efficiency at the desired concentration. In order to optimize solar cell efficiency at the desired concentration and using the above analytical model, the relationship between the five key variables ($V_{oc}$, $J_{sc}$, $R_s$, $R_{sh}$ and $n$) and grid pattern needs to be established. For the Al-BSF cell structure used in this study, $R_{sh}$ and $n$ are assumed near ideal with values of 3000 $\Omega$-cm$^2$ and 1, respectively. Model uses a modeled or measured $J_{sc}$ value under one sun with known grid design. For this section, we used measured one-sun $J_{sc}$ =36.6 mA/cm$^2$ and $V_{oc}$ =622 mV with

metal coverage of 6.8%. Grid design is then changed for the concentrator cell and $J_{sc}$ for different grid was calculated using equation (45) because of its proportionality with un-metallezed area. $V_{oc}$ is calculated using equation (46) by assuming constant $J_o$ for different grid patterns in this study. First, $J_{sc}$ and $V_{oc}$ values at one sun were generated for different grid patterns, as shown in Table 4. Note that grid pattern or metal coverage was affected by changing the grid spacing for a given finger width. Series resistance is the key to achieving high efficiency and dictating the concentration at which highest efficiency will be achieved. Series resistance represents the compounded effect of bulk resistance, emitter sheet resistance, contact resistance, grid resistance and bus resistance. The relationship between $R_s$ and the grid pattern (finger length and spacing) is described by equations (47) to (52) [88] and the measured series resistance related parameters of our one sun cells used in this research, as listed in Table 5. For this work, we used Dupont 16A silver paste for the front grid in combination with widely used $POCl_3$ diffused ∼60 Ω/sq emitter and full Al-BSF as a reference cell with very simple $n^+$-p-$p^+$ structure. The probes to contact busbar in our light IV tester were separated by 5 mm. Using the parameters in Table 5 and equations (47) to (52), $R_s$ (mΩ-cm$^2$) and its various components for different finger spacing are calculated and summarized in Table 6.

**Table 4:** Calculated $J_{sc}$ and $V_{oc}$ under one sun for different finger spacing

| Finger spacing (mm) | Metal coverage | Uncovered area | $J_{sc}$ (mA/cm$^2$) | $V_{oc}$ (mV) |
|---|---|---|---|---|
| 2.48 | 4.4% | 95.6% | 37.5 | 623 |
| 2.26 | 4.9% | 95.1% | 37.3 | 623 |
| 2.00 | 5.5% | 94.5% | 37.1 | 622 |
| 1.79 | 6.1% | 93.9% | 36.8 | 622 |
| 1.63 | 6.8% | 93.2% | 36.6 | 622 |
| 1.49 | 7.4% | 92.6% | 36.4 | 622 |
| 1.37 | 8.0% | 92.0% | 36.1 | 622 |
| 1.27 | 8.7% | 91.3% | 35.9 | 621 |
| 1.16 | 9.5% | 90.5% | 35.5 | 621 |
| 1.02 | 10.8% | 89.2% | 35.0 | 621 |

**Table 5:** Experimentally measured parameters for Dupont 16A screen-printed contacts

| Parameters | Screen-Printed |
|---|---|
| Busbar length ($b$) (mm) | 52 |
| Busbar width (mm) | 2 |
| Probes spacing in IV tester($c$) (mm) | 5 |
| Finger length (mm) | 70 |
| Finger width ($W_{finger}$) ($\mu$m) | 110 |
| Effective finger length ($a$) (mm) | 35 |
| Busbar resistance ($R_{bus-m}$) (m$\Omega$) | 29.1 |
| Finger line resistance ($R_{fl-m}$) (m$\Omega$/mm perline) | 19.7 |
| [1]Specific contact resistance ($R_{con-m}$) (m$\Omega$-cm$^2$) | 3.42 |
| Sheet resistacne ($R_{sh-m}$) ($\Omega$/sq) | 61.6 |
| Wafer resistivity ($R_{w-m}$) ($\Omega$-cm) | 2 |
| Wafer thickness ($t$) ($\mu$m) | 170 |

[1]The specific contact resistance is calculated from the total finger width.

**Table 6:** Calculated $R_s$ and its components for different finger spacing

| Finger spacing (mm) | Busbar $R_s$ (m$\Omega$-cm$^2$) | Fingers $R_s$ (m$\Omega$-cm$^2$) | Contact $R_s$ (m$\Omega$-cm$^2$) | Emitter $R_s$ (m$\Omega$-cm$^2$) | Substrate $R_s$ (m$\Omega$-cm$^2$) | Total $R_s$ (m$\Omega$-cm$^2$) |
|---|---|---|---|---|---|---|
| 2.48 | 0.4 | 199.2 | 77.0 | 314.8 | 8.5 | 600 |
| 2.26 | 0.4 | 181.8 | 70.3 | 262.4 | 8.5 | 624 |
| 2.00 | 0.4 | 160.9 | 62.2 | 205.3 | 8.5 | 437 |
| 1.79 | 0.4 | 144.2 | 55.8 | 165.0 | 8.5 | 374 |
| 1.63 | 0.4 | 130.7 | 50.6 | 135.6 | 8.5 | 326 |
| 1.49 | 0.4 | 119.5 | 46.2 | 113.3 | 8.5 | 288 |
| 1.37 | 0.4 | 110.1 | 42.6 | 96.1 | 8.5 | 258 |
| 1.27 | 0.4 | 102.0 | 39.5 | 82.6 | 8.5 | 233 |
| 1.16 | 0.4 | 92.9 | 35.9 | 68.5 | 8.5 | 206 |
| 1.02 | 0.4 | 82.0 | 31.7 | 53.4 | 8.5 | 176 |

The factor 4 in the denominator of equation (51) accounts for resistivity change due to high level injection under 20X. This was partly supported by PC1D model simulations under $V_{oc}$ condition. The same equation can be also used under low concentration as an approximation, because substrate resistance had no appreciable impact on $R_s$ and cell performance. Lowering it further will not change the outcome. This simple approximation is validated by the good fit between experimental and model data in Figure 24, Figure 26 and Figure 29 in the concentration range of 1-20X.

$$J_{sc} \propto \left(1 - \frac{W_{finger}}{spacing}\right) \tag{45}$$

$$V_{oc} = \frac{kT}{q} ln\left(\frac{J_{sc}}{J_o} + 1\right) \tag{46}$$

$$R_{busbar} = \frac{1}{3} \cdot a \cdot \left(\frac{c}{2}\right)^2 \cdot \frac{R_{bus-m}}{b} \tag{47}$$

$$R_{finger} = \frac{1}{3} \cdot a^2 \cdot spacing \cdot R_{fl-m} \tag{48}$$

$$R_{contact} = \frac{R_{con-m}}{W_{finger}} \cdot spacing \tag{49}$$

$$R_{emitter} = \frac{1}{3} \cdot \left( \frac{spacing}{2} \right)^2 \cdot R_{sh-m} \tag{50}$$

$$R_{substrate} = \frac{R_{w-m}}{4} \cdot t \tag{51}$$

$$R_s = R_{busbar} + R_{finger} + R_{contact} + R_{emitter} + R_{substrate} \tag{52}$$

### 4.2.1 Use of the Analytical Model to Calculate Highest Achievable Efficiency at Various Concentration from a Given Cell Technology and Structure

With the five predetermined values of $V_{oc}$ (Table 4), $J_{sc}$ (Table 4), $R_s$ (Table 6), $R_{sh}$ (assumed to be 3000 $\Omega$-cm$^2$) and $n$ (assumed to be 1), the cell efficiency is calculated at different suns using the analytical model in Section 4.1 (equations 37-44) for different grid pattern or spacing, as shown in Table 7. The finger width and length were fixed at 110 $\mu$m and 70 mm, respectively, and spacing was varied from 1.02 to 2.48 mm. As expected, change in finger spacing (or the number of lines) results in change in peak efficiency as well as the concentration at which the peak occurs. For example, Table 7 shows that 1.02 mm finger spacing results in a peak efficiency of 18.6% at 5X while spacing of 1.63 mm produces a maximum efficiency of 18.8% at 3X for the given cell structure.

**Table 7:** Calculated cell efficiency as a function of finger spacing and concentration

| Spacing (mm) | $R_s$ ($\Omega$-cm$^2$) | $J_{sc}$ (mA/cm$^2$) | $V_{oc}$ (mV) | 1X $\eta$ (%) | 3X $\eta$ (%) | 4X $\eta$ (%) | 5X $\eta$ (%) | 6X $\eta$ (%) | 8X $\eta$ (%) | 10X $\eta$ (%) | 12X $\eta$ (%) | 14X $\eta$ (%) | 15X $\eta$ (%) | 17X $\eta$ (%) | 20X $\eta$ (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2.48 | 595 | 37.5 | 623 | 18.6 | 18.3 | 17.9 | 17.4 | 16.8 | 15.7 | 14.5 | 13.2 | 11.9 | 11.3 | 9.9 | 7.9 |
| 2.26 | 518 | 37.3 | 623 | 18.7 | 18.5 | 18.2 | 17.7 | 17.3 | 16.3 | 15.3 | 14.2 | 13.1 | 12.6 | 11.5 | 9.8 |
| 2.00 | 432 | 37.1 | 622 | 18.6 | 18.7 | 18.4 | 18.1 | 17.8 | 17.1 | 16.2 | 15.4 | 14.5 | 14.1 | 13.2 | 11.8 |
| 1.79 | 369 | 36.8 | 622 | 18.6 | 18.8 | 18.6 | 18.4 | 18.1 | 17.5 | 16.9 | 16.2 | 15.5 | 15.1 | 14.4 | 13.2 |
| 1.63 | 321 | 36.6 | 622 | 18.5 | 18.8 | 18.7 | 18.5 | 18.3 | 17.9 | 17.3 | 16.8 | 16.2 | 15.9 | 15.2 | 14.3 |
| 1.49 | 283 | 36.4 | 622 | 18.4 | 18.8 | 18.8 | 18.6 | 18.5 | 18.1 | 17.7 | 17.2 | 16.7 | 16.4 | 15.9 | 15.1 |
| 1.37 | 253 | 36.1 | 622 | 18.3 | 18.8 | 18.8 | 18.7 | 18.6 | 18.3 | 17.9 | 17.5 | 17.1 | 16.8 | 16.4 | 15.7 |
| 1.27 | 228 | 35.9 | 621 | 18.2 | 18.7 | 18.7 | 18.7 | 18.6 | 18.4 | 18.0 | 17.7 | 17.3 | 17.1 | 16.7 | 16.1 |
| 1.16 | 201 | 35.5 | 621 | 18.0 | 18.6 | 18.7 | 18.7 | 18.6 | 18.4 | 18.2 | 17.9 | 17.6 | 17.4 | 17.1 | 16.6 |
| 1.02 | 171 | 35.0 | 621 | 17.8 | 18.5 | 18.5 | 18.6 | 18.5 | 18.4 | 18.3 | 18.0 | 17.8 | 17.7 | 17.4 | 17.0 |
| Highest Achievable Efficiency | | | | 18.7 | 18.8 | 18.8 | 18.7 | 18.6 | 18.4 | 18.3 | 18.0 | 17.8 | 17.7 | 17.4 | 17.0 |

Besides the peak efficiency at each spacing, this approach also gives the Highest Achievable Efficiency (HAE) at the desired concentration and the corresponding

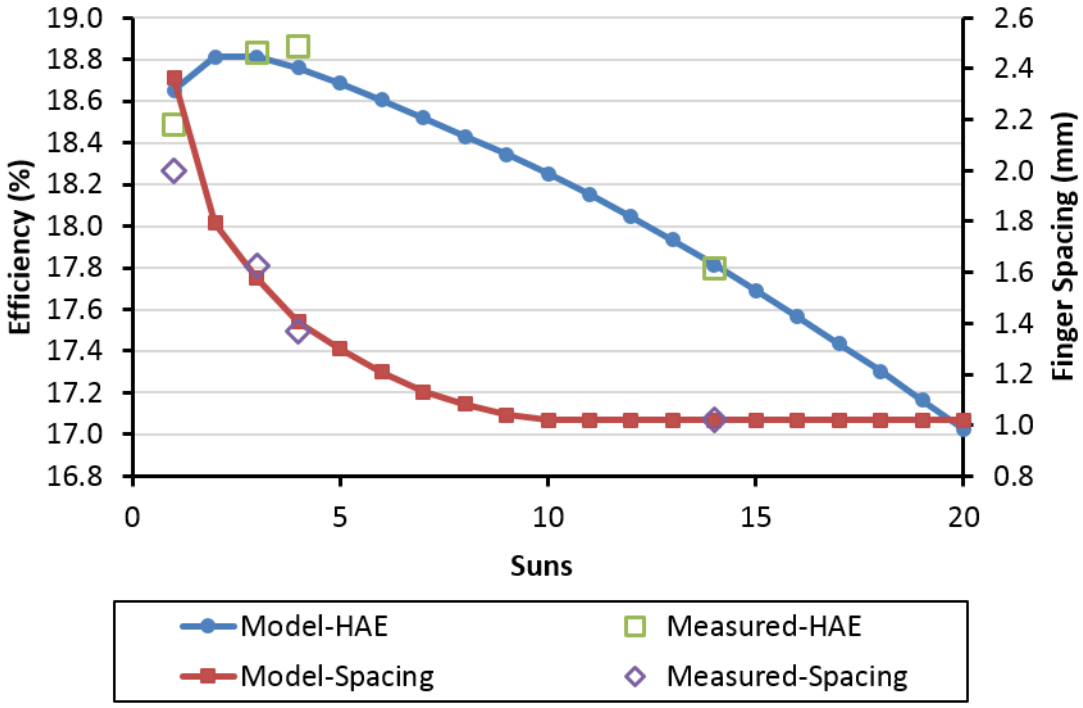



**Figure 24:** Modeled HAE curve and the corresponding finger spacing for the reference technology as a function of concentration. Four data points show a good match between the model and the experimental data. Measured cell efficiency as function of suns for different finger spacing are shown in Figure 25.

spacing. This is done by tabulating the maximum efficiency for each sun in Table 7 and the corresponding grid spacing, as shown in Figure 24. This graph quantifies the HAE at any given sun (blue curve) from this technology and the required finger spacing (red curve) to achieve that. For example, Figure 24 shows that this basic/reference cell technology (18.3% cell at 1X) with full Al-BSF can produce a maximum efficiency of 18.8% at 3X with a finger spacing of 1.58 mm, where 0.4% of efficiency improvement is from aperture area and 0.1% from concentrated light and grid design. Note that this screen-printed cell technology and structure can also give an efficiency of 17.0% at 20X with a finger spacing of 1.02 mm.

## *4.3 Concentrator Cell Fabrication to Validate the Model and Methodology*

In order to validate the above calculations, we fabricated concentrator cells with four different finger spacings of 2.00, 1.63, 1.37, and 1.02 mm on large area 239 $cm^2$, 170 $\mu$m thick p-type boron doped, ~2 Ω-cm Cz wafers. An industrial type cell process sequence was used which involved: (a) saw damage removal in a heated KOH solution, (b) alkaline texturing of both sides, (c) standard $POCl_3$ diffusion to create ~60 Ω/sq $n^+$ emitter, (d) chemical edge isolation, (e) PECVD $SiN_x$ deposition, (f) screen printing of Dupont 16A silver paste on the front and commercial Al paste to form full area Al BSF and back contact, (g) contact firing in a belt furnace, (h) laser dicing into six 52×78 mm cells.

**Table 8:** Modeled and measured $R_s$, $J_{sc}$, and $V_{oc}$ under one sun for 35 mm effective finger length

| Finger Spacing (mm) | 2.00 | 1.63 | 1.37 | 1.02 |
|---|---|---|---|---|
| Modeled $R_s$ (mΩ-$cm^2$) | 437 | 326 | 258 | 176 |
| Measured $R_s$ (mΩ-$cm^2$) | 471 | 306 | 230 | 199 |
| Relative Diff | -7.2% | 6.5% | 12.2% | -11.6% |
| Modeled $J_{sc}$ (mA/$cm^2$) | 37.1 | 36.6 | 36.1 | 35 |
| Measured $J_{sc}$ (mA/$cm^2$) | 37.3 | 36.6 | 36.2 | 35.1 |
| Relative Diff | -0.5% | 0.0% | -0.3% | -0.3% |
| Modeled $V_{oc}$ (mV) | 622 | 622 | 622 | 621 |
| Measured $V_{oc}$ (mV) | 623 | 622 | 620 | 622 |
| Relative Diff | -0.2% | 0.0% | 0.3% | -0.2% |

Cells were measured with Sinton concentrator tester [89], which uses Suns-$V_{oc}$ method to extract the $R_s$ value [90]. The modeled and measured $R_s$, $J_{sc}$, and $V_{oc}$ values at 1 sun are listed in Table 8, which shows a very good agreement. We have used the average of at least 3 cells for each condition. Figure 25 shows the measured efficiency versus suns curves for the 4 different finger spacing. The data showed maximum efficiency of 18.5% at 1X, 18.8% at 3X, 18.9% at 4X and 17.7% at 15X for a finger spacing of 2.00, 1.63, 1.37 and 1.02 mm, respectively. These four data points in Figure 24 show an excellent match between experimental data and model

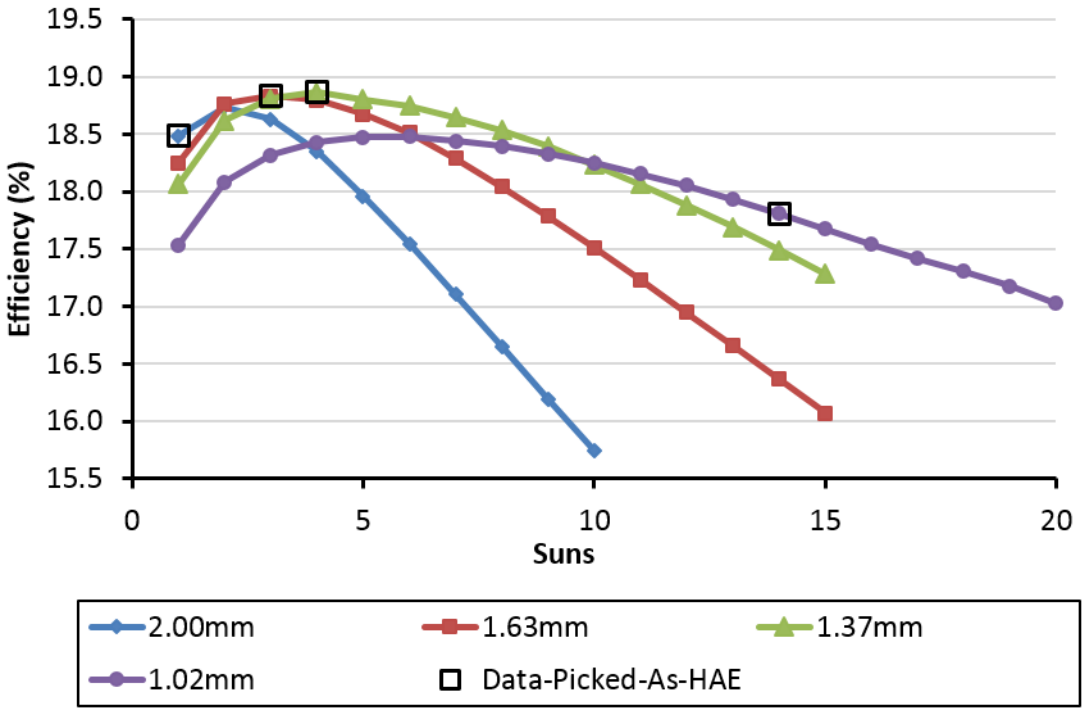



**Figure 25:** Measured cell efficiency as function of suns for different finger spacing. The circled data points were picked as HAE.

predictions.

## *4.4 Modeling and Experimental Validation of the Impact of Finger Length on the Highest Achievable Efficiency Curve*

After establishing the above methodology and validating it with cell fabrication, the next step was to apply this concept to attain higher concentrator cell efficiencies using screen-printed contacts. It has been shown that finger length plays an important role in the performance of screen-printed low to medium concentrator solar cells, especially at higher concentration [9]. Therefore, we first extended our analysis to account for this effect for the same screen-printed cell design and structure. Two effective finger lengths, 35 mm (reference) and 25 mm (reduced) were selected, which represent total finger length of 70 mm and 50 mm for cells with two busbars, respectively. Next,

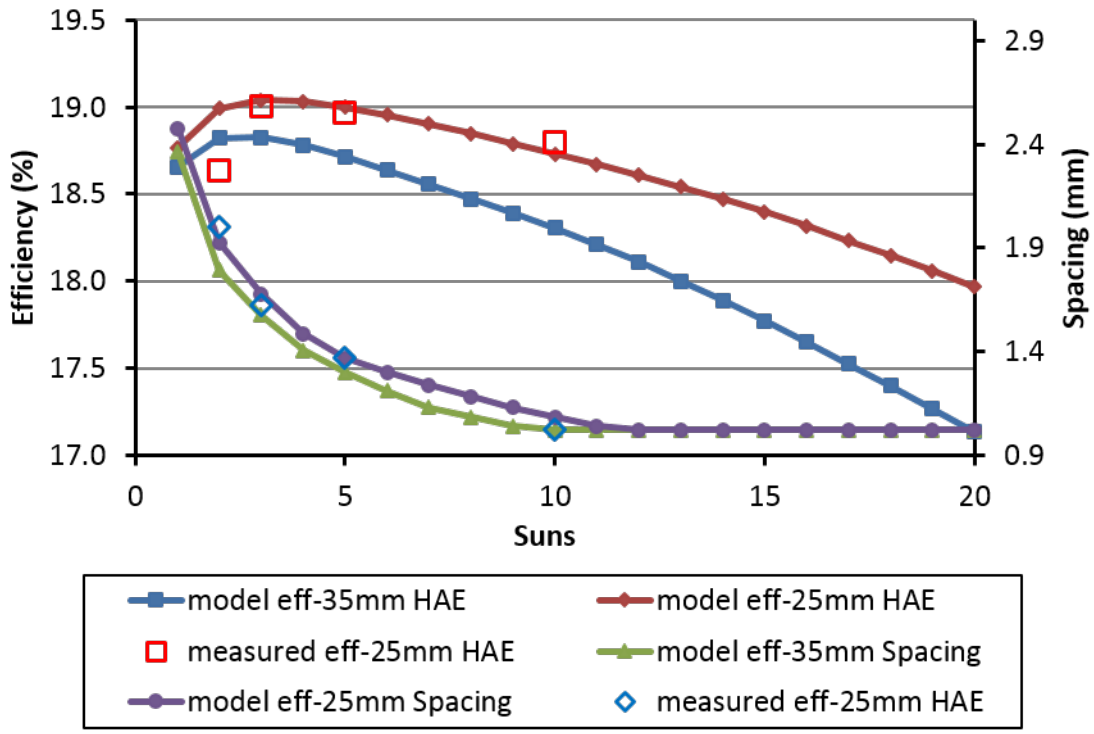



**Figure 26:** Calculated HAE as functions of concentration and number of fingers with different effective finger lengths (reference: 35 mm and reduced: 25 mm). The experimental data for 25 mm effective finger length cells are also shown for validation.

the same modeling steps were applied to extract the HAE curve as functions of light intensity and number of fingers. Model calculations in Figure 26 reveal that reducing the finger length for this metal paste can enhance absolute efficiency by 0.2-0.9% depending on the concentration (1-20X). Calculations show quantitatively that 25 mm effective finger length is superior to the reference 35 mm finger length over the entire range (1-20X) due to the reduced finger line resistance. The best modeled efficiency is 19.0% at 2-5X, improving from 18.3% at 1X, where 0.4% of efficiency improvement is from aperture area and 0.3% is from concentrated light and corresponding finger design. To validate the above model calculations, we fabricated cells with one busbar with effective finger length of 25 mm, which is equivalent to cells with 50 mm finger length with two busbars (Figure 27). Figure 28 shows the measured efficiency versus suns curves for the 4 different finger spacing with reduced finger length using the

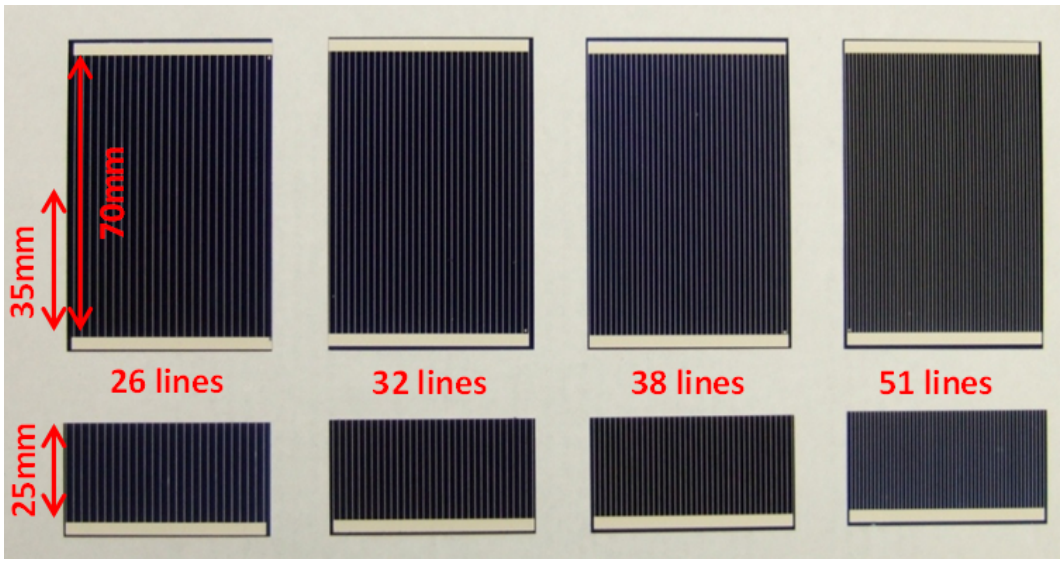



**Figure 27:** Picture of the finished two busbar cells with 70 mm finger length (35 mm effective finger length) and one busbar cell with 25 mm effective finger length.

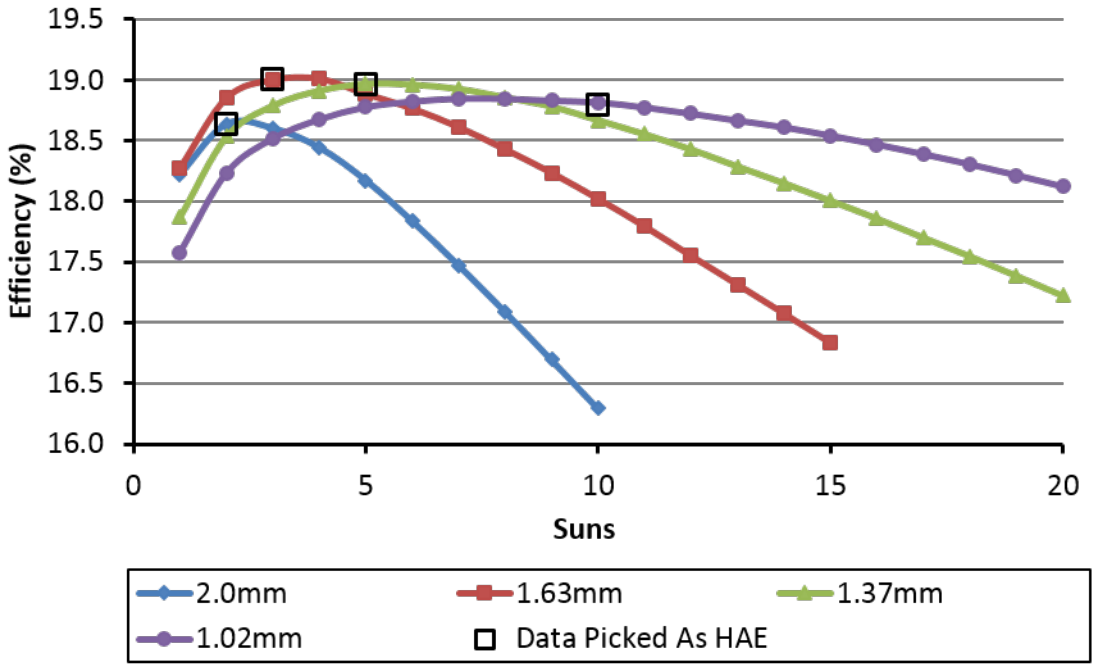



**Figure 28:** Measured cell efficiency as function of suns for different finger spacing (25 mm effective finger length). The circled data points were picked as HAE.

reference technology, which gives a maximum efficiency of 18.6% at 2X, 19.0% at 3X, 19.0% at 5X and 18.8% at 10X using a finger spacing of 2.00, 1.63, 1.37 and 1.02 mm,

respectively. This information when marked on Figure 26 (square points) shows an excellent match between the model and experimental data.

## *4.5 Demonstration of High Efficiency ≥20% Efficient Direct Paste-printed Concentrator Si Solar Cell*

Section 4.4 showed that reducing the finger length improves the HAE curve, but was only able to get to 19.0% efficiency. This is because reference screen-printed technology at that time (2009) could not print less than 75-100 $\mu$m line width. Current screen-printed line width has come down to ~60 $\mu$m. Therefore, the next step was to achieve ≥20% efficiency by improving the contact technology achieved with narrow (~50 $\mu$m) grid lines. This was done by implementing a technology called extrusion or direct printing of Ag paste. We were successful in printing 50 $\mu$m wide direct

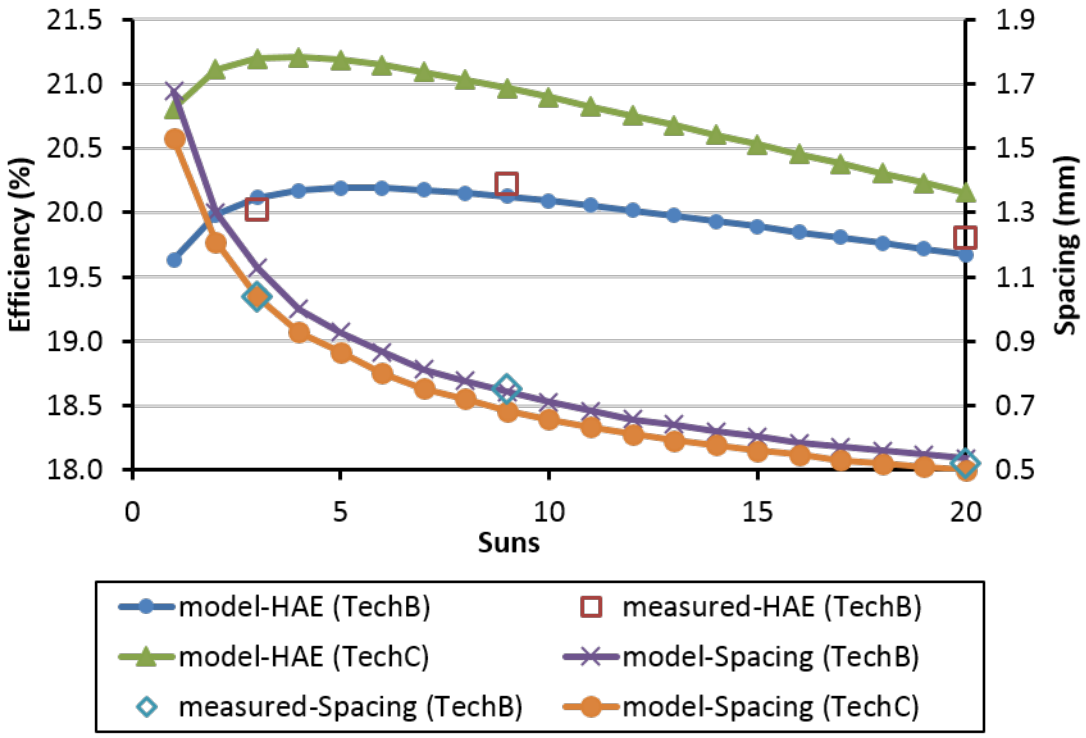



**Figure 29:** The roadmap to ≥20% efficient metal printed concentrator Si solar cells. Tech B: 50 $\mu$m line width and full Al-BSF. Tech C: PERC cell design with 50 $\mu$m line width. More detailed parameters for Tech B and Tech C are listed in Table 9. The experimental data for Tech B is also shown.

paste-printed fingers as opposed to 110 $\mu$m wide screen-printed lines in the previous section. Direct printing work was done in collaboration with nScrypt Corp. More details about the direct printing technology can be found in [91]. The cell fabrication process was essentially the same as in Section 4.3, except for the slightly lighter doped emitter ($\sim$70 $\Omega$/sq) and the thinner printed fingers ($\sim$50 $\mu$m). Next, we applied our methodology to design the appropriated grid pattern for achieving $\geq$20% cell. First we fabricated 1 sun cells using this 50 $\mu$m technology which improved the efficiency from 18.3 to 19.0%. From the one sun cell parameters along with the detailed paste parameters in Table 9 (column Tech B), concentrator cell efficiencies were calculated as shown in Figure 29. Modeled HAE curve in Figure 29 (Tech B) for this improved direct metal printing technology showed that 20.1% efficient cells can be achieved at 9X with 0.74 mm finger spacing, improving from 19.0% under 1X. This absolute 1.1% efficiency improvement resulted from 0.6% increase from aperture area and 0.5% from concentrated light and corresponding finger design.

To validate these model calculations, concentrator cells were fabricated with a finger spacing of 1.04, 0.75 and 0.52 mm, respectively. The experimental efficiency curves as a function of suns for the three cells are shown in Figure 30. Figure 30 shows that the improved direct paste printing technology with 50 $\mu$m wide lines can give a maximum efficiency of 20.0% at 3X, 20.2% at 9X and 19.8% at 20X with a finger spacing of 1.04, 0.75 and 0.52 mm, respectively. Figure 29 (Tech B) shows that this is in excellent agreement with the modeled HAE curve. Note that 20.2% efficiency achieved in this study at 9X was one of the highest efficiency for low-medium concentrator Si solar cell with metal printed contacts at that time.

## *4.6 Roadmap to $\geq$21% Efficient Screen-printed Concentrator Si Solar Cell*

After achieving $\geq$20% efficient cells by improving cell design and screen printing parameters (Tech B), we applied this methodology to obtain guidelines for $\geq$21%

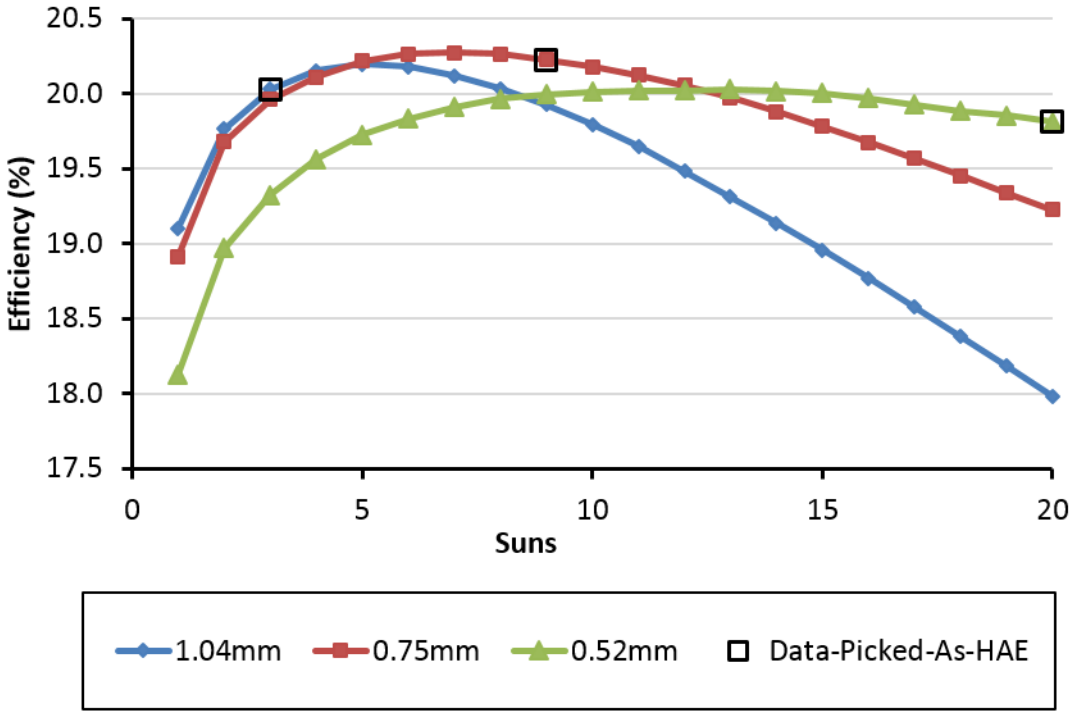



**Figure 30:** Measured cell efficiency as function of suns for different finger spacing with 50 $\mu$m wide finger. The circled data points were picked as HAE.

**Table 9:** Experimental constants from Dupont 16A Ag Paste and nScrypt fingers with $POCl_3$ diffused emitter and predicted constants for nScrypt back-passivated PERC cell

| Cell Parameters | [1]Tech A 110 $\mu$m line width with full Al-BSF | Tech B 50 $\mu$m line width with full Al-BSF | Tech C 50 $\mu$m line width with PERC |
|---|---|---|---|
| $V_{oc}$ at 1 sun (mV) | 622 | 622 | 657 |
| $J_{sc}$ at 1 sun (mA/cm$^2$) | 36.6 | 37.4 | 39.5 |
| Metal coverage (%) | 6.75 | 6.67 | 2.93 |
| n-factor | 1 | 1 | 1.1 |
| Rshunt ($\Omega$-cm$^2$) | 3000 | 3000 | 3000 |
| Busbar length (mm) | 52 | 52 | 52 |
| Finger length (mm) | 50 | 50 | 50 |
| Finger spacing (mm) | 1.63 | 0.75 | 1.71 |
| Wafer resistivity ($\Omega$-cm) | 2 | 2 | 2 |
| Wafer thickness ($\mu$m) | 170 | 170 | 170 |
| Busbar resistance (m$\Omega$) | 29.1 | 29.1 | 29.1 |
| Finger line resistance (m$\Omega$/mm perline) | 19.7 | 28.2 | 28.2 |
| [2]Specific contact resistance (m$\Omega$-cm$^2$) | 3.42 | 2.18 | [3]2.18 |
| sheet resistacne ($\Omega$/sq) | 61.6 | 68 | 100 |
| Finger width ($\mu$m) | 110 | 50 | 50 |

[1]Tech A is the cells as in Section 4.4. [2]The Specific contact resistance is calculated by the total finger width, not transfer length as in [88]. [3]Predicted value.

low-medium concentrator cells. Technology C in Table 9 and Figure 29 together show that ≥21% cells can be achieved by changing the cell structure from simple full Al-BSF on the back to PERC (passivated emitter and rear cell) [92], which uses rear dielectric back passivation and local BSF on the back structure. In this case, we used the experimental data from [93], which has PERC cell efficiency of 20.2% at 1X and $V_{oc}$, $J_{sc}$, and $FF$ of 657 mV, 38.4 mA/cm$^2$, and 80.0%, respectively. Then we applied our methodology to calculate the highest achievable concentrator cell efficiency for this technology. Model calculations gave a highest efficiency of 21.2% at 4X with a finger spacing of 0.93 mm using 16A paste and 25 mm effective finger length. Figure 31 shows that 1% increase in absolute efficiency resulted from 0.6% increase from the aperture area and 0.4% given from the concentrated light and grid design. The model also shows that 20.2% PERC cell efficiency at 20X is achievable from this technology with a finger spacing of 0.52 mm.

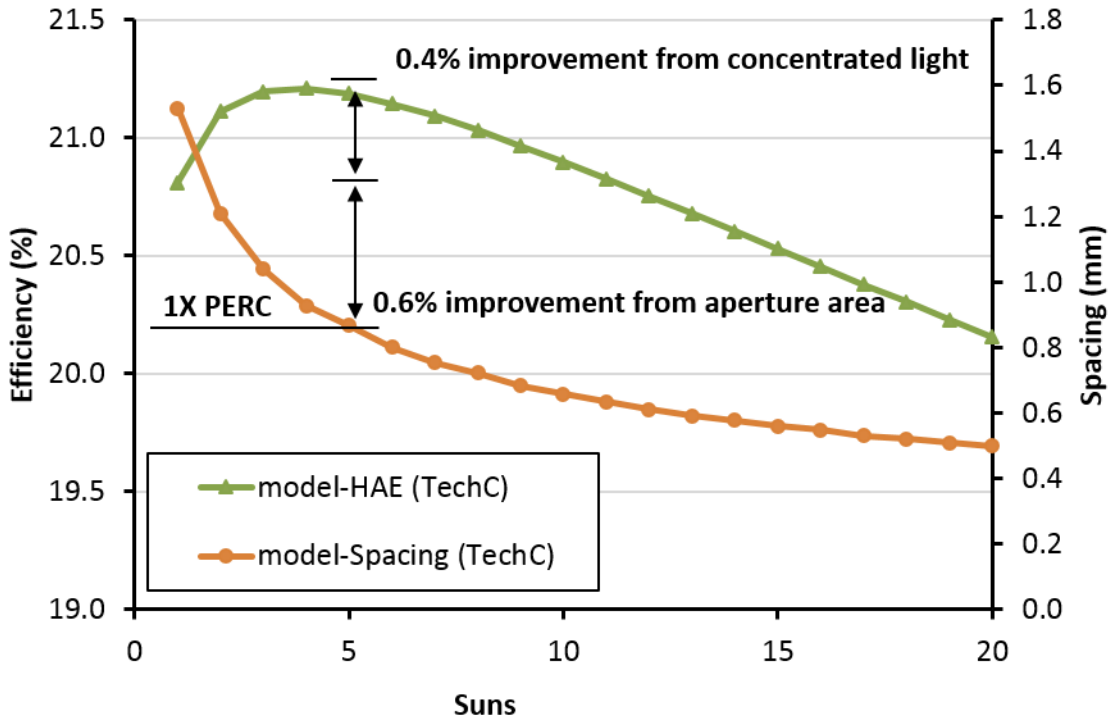



**Figure 31:** Efficiency improvement from 1X PERC cell to low-medium concentrator PERC cell.

## *4.7 Summary*

In this task, we have developed a methodology and applied it to generate Highest Achievable Efficiency (HAE) curve at various concentration (1-20X) by optimizing the front metal pattern design of screen-printed concentrator Si solar cells. The model first calculates $R_s$ and its components as a function of finger spacing with given finger length using the measured contact related experimental parameters. $V_{oc}$ and $J_{sc}$ at 1 sun for different finger spacings are then determined from a measured reference cell data with known metal coverage. This allows the analytical model to calculate efficiency as a function of concentration from which the HAE curve as a function of finger spacing and concentration is extracted. The model was validated by fabricating and analyzing concentrator Si solar cells. At the start of this research, a commercial baseline screen-printed technology was used to produce 18.3% efficient cells at one sun. It was demonstrated that this efficiency can be increased to 19.0% at 4-5X with 1.63 mm finger spacing for 25 mm effective finger length. In addition, an efficiency of 18.0% at 20X was also demonstrated. It was found that efficiency of these cells was limited by the 110 $\mu$m wide screen-printed fingers. Therefore, a new extrusion printing technology was implemented to print 50 $\mu$m wide Ag lines. This produced 19.0% cells at one sun and 20.2% efficient cell at $\sim$9X with 25 mm long effective fingers and spacing of 0.72 mm. This was in excellent agreement with the model calculations of the HAE at a given concentration for this technology. Following the guide of HAE curve, an efficiency of 19.8% at 20X was demonstrated for this technology with finger spacing reduced to 0.52 mm. This represents one of the highest efficiency direct metal printed low-medium concentrator cells at the time. Finally, a roadmap to achieve $\geq$21% 3-5X efficient concentrator Si solar cell was developed for a 20.2% one-sun advanced PERC cell structure using direct printed lines.

# CHAPTER V

# STRATEGY AND VARIOUS CELL STRUCTURES INVESTIGATED ON EPITAXIALLY GROWN SI SUBSTRATE

This Chapter describes various promising cell structures designed and fabricated on epi-grown Si substrates in this research. Chapters VI to IX (Tasks 2 to 5) deal with solar cells made on epitaxially grown Si (epi-Si) wafers with and without built-in junctions or doped layers to reduce the Si material and cell processing costs while achieving higher cell efficiency. In Chapter VI (Task 2), epi-Si cells were made using epitaixal wafer equivalent (EpiWE) structure (Figure 32 a), which involves eptiaxial

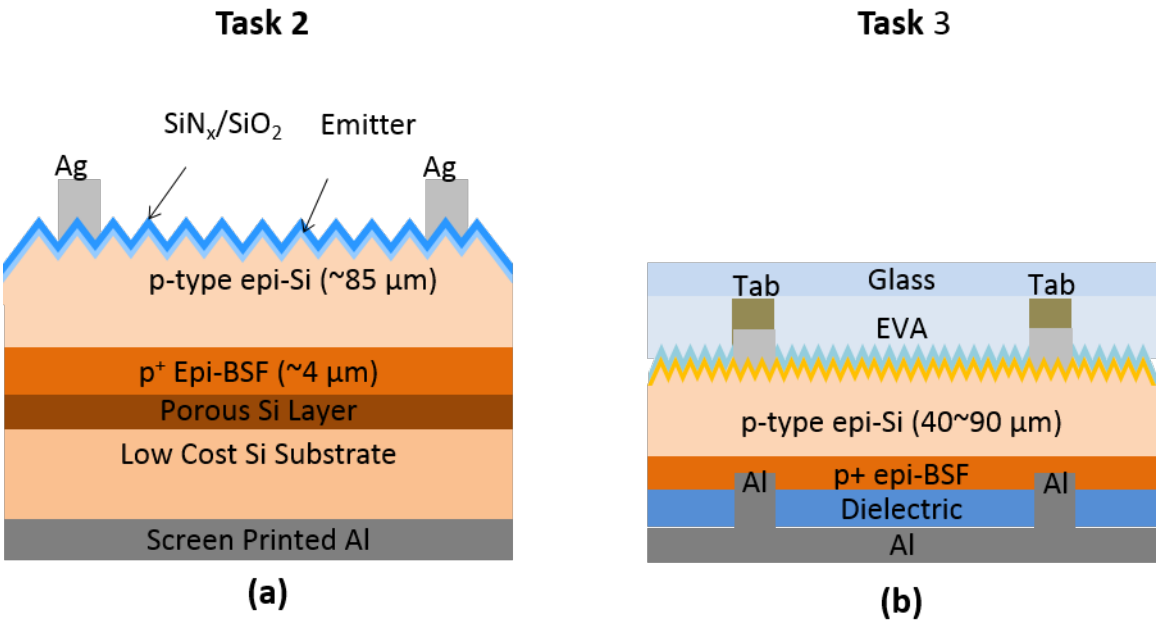



**Figure 32:** (a) Schematic cross-section of a thin epi-Si solar cell using Epitaxial Wafer Equivalent (EpiWE) structure with PSI as back reflector. (b) Schematic cross-section of a thin epi-Si solar cell using layer transfer process to glass/EVA carrier.

growth of Si active layers on top of a porous Si (PSI) formed on a highly doped Si substrate. Reasonably good efficiency numbers were achieved. However, low-cost Si substrate was part of the EpiWE structure so full Kerf loss saving could not be realized. To solve this problem, in Chapter VII (Task 3), thin epi-Si cells were fabricated using novel layer transfer process to a glass/EVA carrier (Figure 32 b). In this approach, Kerf loss is avoided because thin epi-Si wafers are used for cell while the substrate is reused for next epi growth.

Although good cell efficiency numbers were realized with this technology, these thin epi-Si cells posed some challenges in assembly of PV modules with low cost. Therefore, in Task 4 (Chapter VIII), we decided to fabricate high efficiency PERC (passivated emitter and rear cell, Figure 33 a) and PERT (passivated emitter, rear totally-diffused, Figure 33 b) solar cells on free standing thick (∼180 $\mu$m) p-type and n-type Kerfless epi-Si wafers using the layer transfer process.

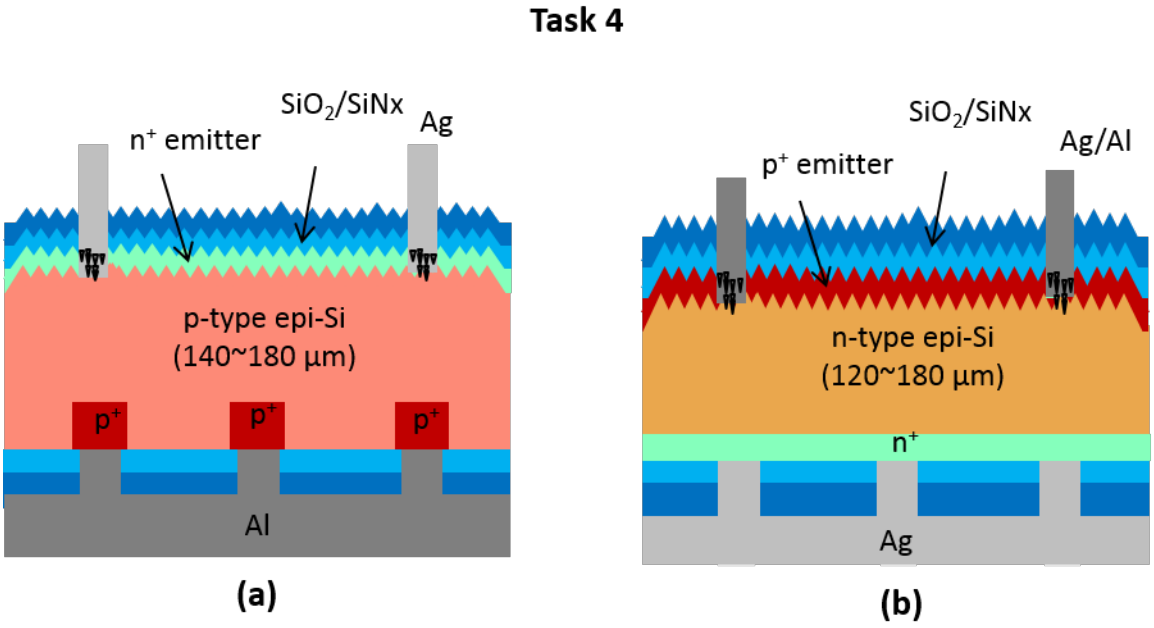



**Figure 33:** (a) Schematic cross-section schematic of a free-standing thick epi-Si p-type PERC solar cell. (b) Schematic cross-section of a free-standing thick epi-Si n-type PERT solar cell.

In Chapter IX (Task 5), we extended the use of epi-Si technology to fabricate p-type PERT solar cells using epi-Si wafers with built-in $p^+$-BSF (Figure 34 a). Finally, we modeled a 3-layer epi-grown PERT cell with epi grown emitter, bulk and BSF (Figure 34 b) that can achieve $\geq$22.7% efficiency with the implementation of selective emitter. All these cell structures are studied in this thesis shown schematically in Figures 32-34.

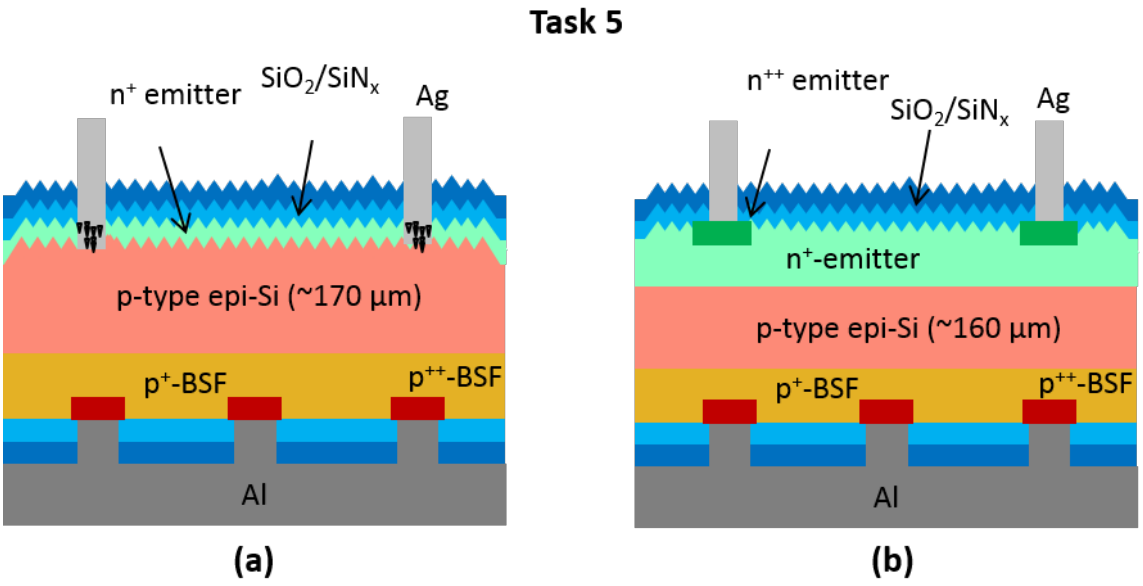



**Figure 34:** (a) Schematic cross-section of an epi-Si p-type PERT solar cell with built-in BSF (b) Schematic cross-section of a 3-layer epi-Si p-type PERT solar cell with selective emitter.

# CHAPTER VI

# TASK 2: DEVELOPMENT OF SCREEN-PRINTED THIN EPI-SI SOLAR CELL USING EPITAXIAL WAFER EQUIVALENT STRUCTURE

In this Chapter, high efficiency 17.3% screen-printed solar cells were fabricated on 90 $\mu$m thick and 182 cm$^2$ large area epi-Si active layer with PSI back reflector between the epi-Si layer and a low-cost Si substrate using EpiWE structure. A standard industrial cell process was used to produce these best in class cells. The Porous Si (PSI) layer was studied and optimized to serve as an efficient back reflector in the finished device. An effective back surface recombination velocity ($BSRV$) of 90 cm/s and back internal reflectance ($R_b$) of 88% were extracted by PC1D modeling of these EpiWE cells. These values are superior to a standard industrial full Al-BSF Si solar cell where $BSRV$ and $R_b$ values are usually $\geq$200 cm/s and $\sim$65%, respectively. Model calculations showed very little drop in cell efficiency even if the thickness of the active epi-Si layer is reduced to $\sim$30 $\mu$m because of the good light trapping provided by the optimized PSI back reflector.

## *6.1 Porous Si Back Reflector Design and Implementation*

### 6.1.1 Refractive Index Requirement for Efficient Back Reflector

To establish the refractive index for an efficient back reflector, Figure 35 from [94] was used with regular pyramid texture surface on the front and planar back. This figure also shows the incident angles (41.4° and 59.1°) on the back surface. Using Snells law ($n_1 sin\theta_1 = n_2 sin\theta_2$, with $n_1 = 3.55$, $\theta_1 = 41.4°$, and $\theta_2 = 90°$), we determined that the refractive index of the back reflector ($n_2$) needs to be smaller than $\sim$2.35 to

ensure total reflection ($\theta_2 = 90°$) at the Si and back reflector interface. In addition, thickness needs to be larger than ~400 nm for total reflection with reduced losses. Next, we investigated the formation of PSI to achieve the target refractive index.

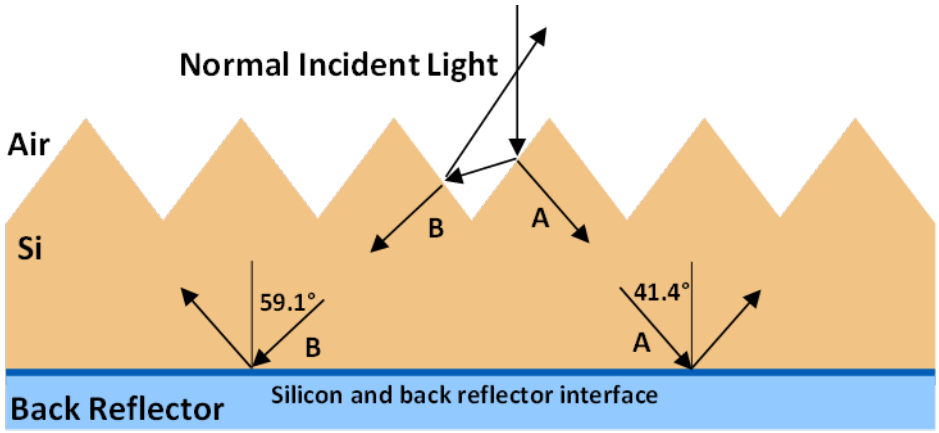



**Figure 35:** The cross-section schematic of 2D approximated light path and cell structure. The angles were calculated with $n_{Si} = 3.55$.

### 6.1.2 Refractive Index as a Function of Porosity of PSI

The refractive index of PSI is known to be a function of Si porosity [95]. Bruggeman and Maxwell Garnett models were used to estimate the PSI refractive index as a function of porosity using equations (53) and (54) [95], where $p$, $n_{si}$ and $n$ are PSI porosity, Si refractive index (3.55) and PSI effective refractive index, respectively. Both models are plotted in Figure 36, with effective refractive index on the y-axis and Si porosity on the x-axis. It is clear that, greater than ~55% porosity is required for PSI effective refractive index to be below 2.35. The higher the porosity, the lower the PSI effective refractive index, and the better the total internal reflection. These guidelines were used in the formation of PSI layer which was formed by anodic etching of the surface of low-cost Si substrate.

$$\text{Bruggeman model,} \quad (1-p)\frac{{n_{si}}^2 - n^2}{{n_{si}}^2 + 2n^2} + p\frac{1-n^2}{1+2n^2} = 0 \tag{53}$$

$$\text{Maxwell Garnett model,} \quad \frac{n^2 - {n_{si}}^2}{n^2 + 2{n_{si}}^2} = p\frac{1-{n_{si}}^2}{1+2{n_{si}}^2} \tag{54}$$

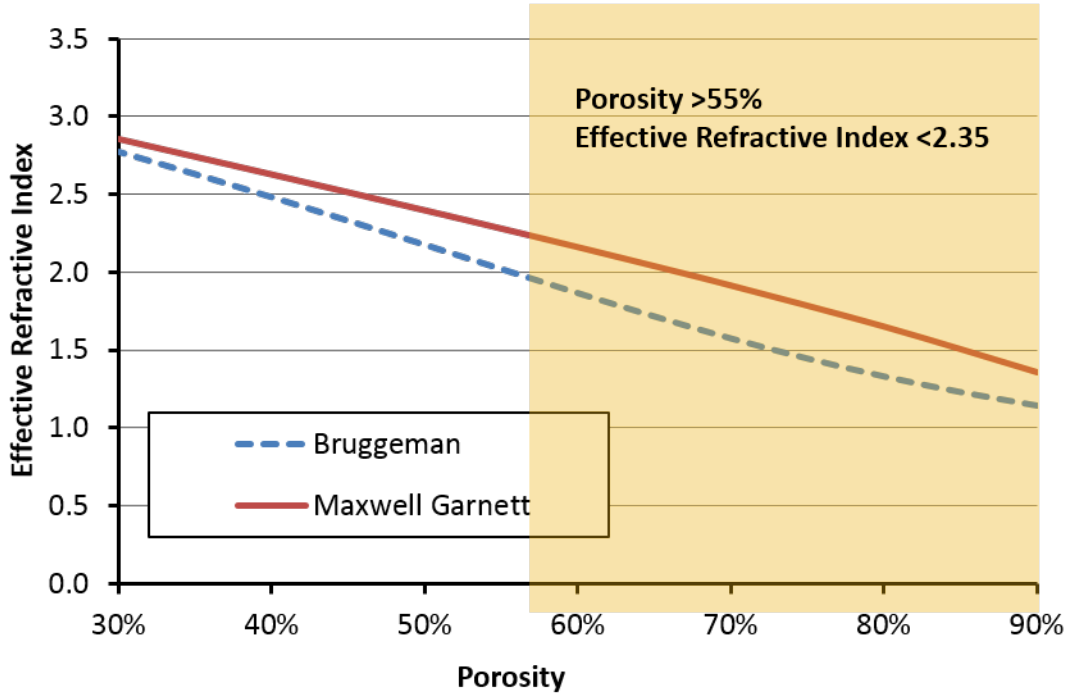



**Figure 36:** PSI effective refractive index as function of PSI porosity calculated by both Bruggeman and Maxwell Garnett Model.

### 6.1.3 PSI Formation to Achieve the Porosity and Refractive Index Targets

Figure 37 shows the SEM picture of our PSI layer. After optimizing the electrochemical etching conditions, a high porosity PSI layer was first formed on top of the Si substrate with a thickness of ~800 nm. Then, a low porosity PSI was formed on top of the high porosity PSI by changing the anodizing current. This enabled the growth of a good quality epi-Si layer. The porosity was estimated to be greater than 80% for the high porosity PSI region, corresponding to a refractive index of ~1.5 (Figure 36). This should ensure total internal reflection at the PSI and Si substrate interface.

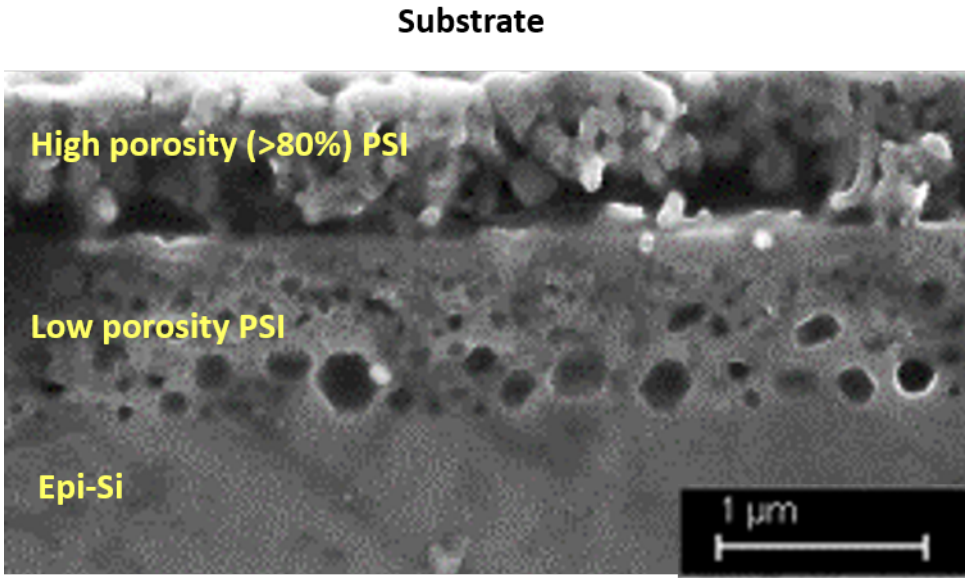



**Figure 37:** SEM picture of our PSI layers.

### 6.1.4 Scattering Factor of PSI and Si Interface

SEM picture in Figure 37 revealed that the interface of PSI and epi-Si was not smooth, with Si and air spatial difference in the order of 100 nm. Therefore, diffuse reflection is expected to occur at the PSI and epi-Si interface. A test sample was prepared with the designed PSI layer in-between the epi-Si and Si substrate. The front surface was polished. We used the procedure in [96] to calculate the scattering factor for characterizing the diffuse reflection. First the total reflectance was measured, which is the sum of specular and diffuse reflection. Then, the total escape reflectance was calculated by subtracting the front surface reflectance (∼34%) from the measured total reflectance (Figure 38). After that, we measured only the diffuse escape reflectance by using a specular light trap in the integrating sphere of Optronic Laboratories spectroradiometric measurement system. The scattering factor was calculated by taking the ratio of diffuse escape reflectance and total escape reflectance at long wavelength, as shown in Figure 38. The data shows ∼99% scattering factor above 1150 nm wavelength. This combined with the low refractive index of the PSI layer should lead to good internal back reflectance as well as very good diffuse reflectance. It has also

been shown that the PSI layer can serve as a diffusion barrier for impurities trying to out diffuse from the lower quality substrate into epi-Si [97, 98]; therefore, lower cost substrate can be used in the EpiWE cell structure without bulk lifetime degradation.

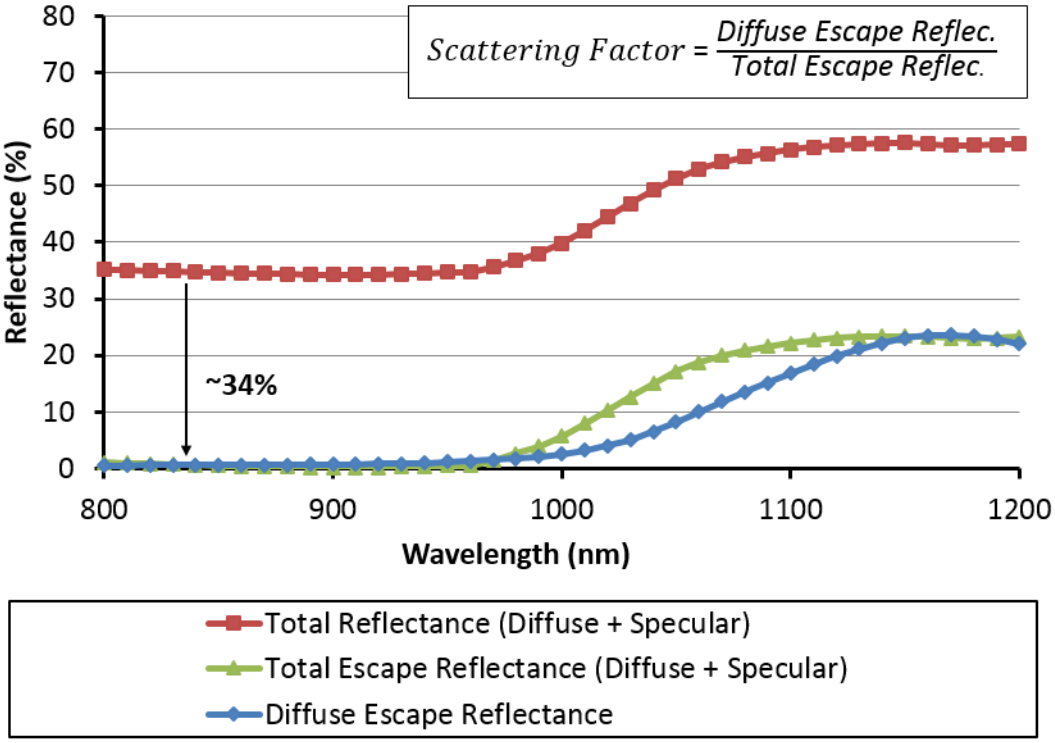



**Figure 38:** Measured and calculated reflectance curves for the test sample with PSI layer in-between the epi-Si and Si substrate. The scattering factor was calculated by taking the ratio of diffuse escape reflectance and total escape reflectance under long wavelength.

## *6.2 Process Flow*

### 6.2.1 Epitaxial Si Layer Deposition by Chemical Vapor Deposition (CVD)

PSI layer was formed by electrochemical etching of the ~750 $\mu$m thick mono-Si substrate. The epi-Si was then deposited on top of the PSI at Crystal Solar Inc. by a CVD process at ~1100 °C. The growth rate was ~4 $\mu$m/min. A thin (~4 $\mu$m) heavily boron doped (~$4\times10^{19}$ cm$^{-3}$) back surface field (BSF) was grown first followed by ~90 $\mu$m thick active absorber layer with a doping of $5\times10^{15}$ cm$^{-3}$ to complete the EpiWE structure, as shown in Figure 39 (a). More details of this CVD epi-Si process

can be found in [99]. The bulk lifetime in the thin active layer was measured to be ~100 $\mu$s by microwave photoconductive decay ($\mu$-PCD) lifetime maps with Semilab WT-2000PV (The surface was passivated by an Iodine/Ethanol solution) [6]. More recently, 780 $\mu$s effective lifetime was reported on optimized 2 Ω-cm p-type epi-Si material [99].

### 6.2.2 Cell Processing

An industrial type cell process sequence was used which involved: (a) random pyramid anisotropic texturing in a KOH based solution, (b) standard RCA clean, (c) standard $POCl_3$ diffusion to create ~65 Ω/sq emitter, (d) phosphosilicate glass (PSG) removal, (e) ~15 nm thermal oxide passivation at ~840°C, (f) PECVD $SiN_x$ antireflection coating, (g) junction isolation by chemical etching. (h) screen printing of commercial silver paste to form 2-busbar "H" grid pattern on the front and commercial Al paste to form full back contact, and (i) contact firing in a belt furnace. The finished cell structure is shown in Figure 39 (b).

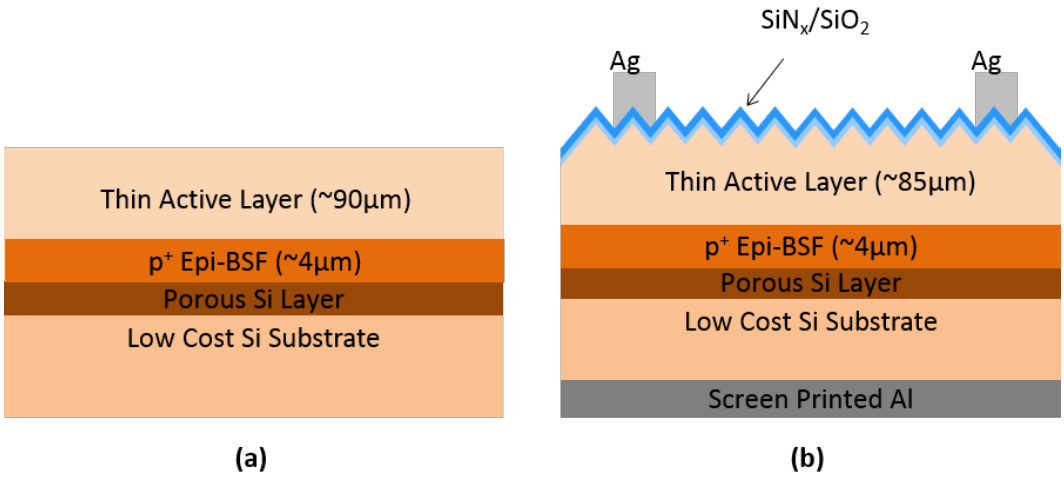
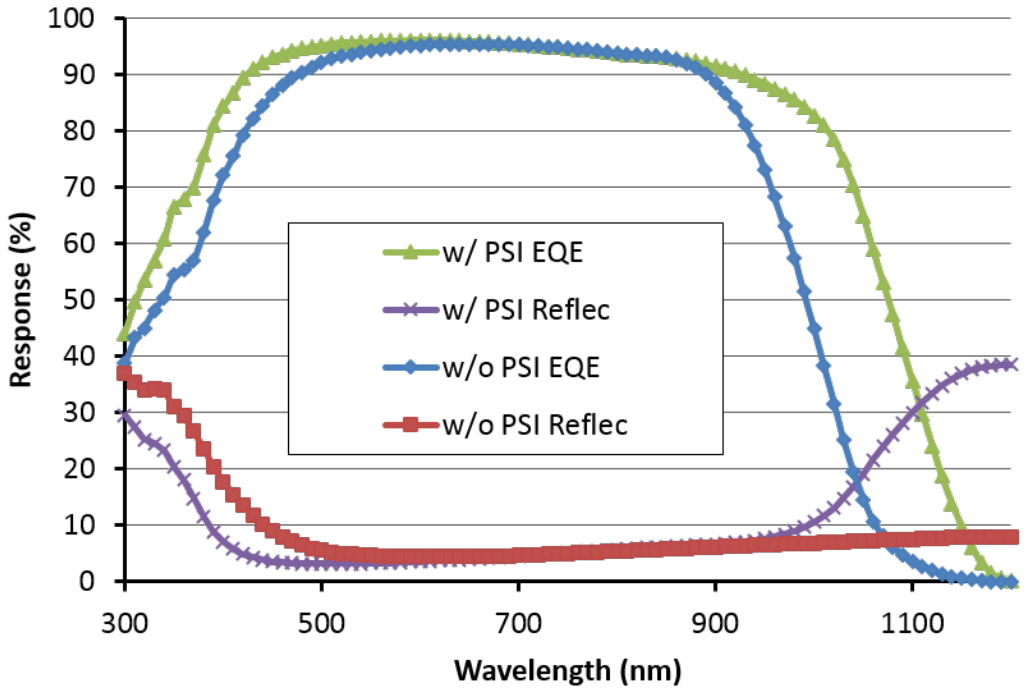



**Figure 39:** (a) The cross-section schematic of Epitaxial Wafer Equivalent (EpiWE) with PSI as back reflector. (b) The cross-section schematic of the finished screen-printed Epi-Si solar cell.

## *6.3 Modeling and Analysis of EpiWE Cell with PSI between the Epi-Si Layer and Si Substrate*

### 6.3.1 Comparison between the Epi-Si Cells with and without PSI Back Reflector

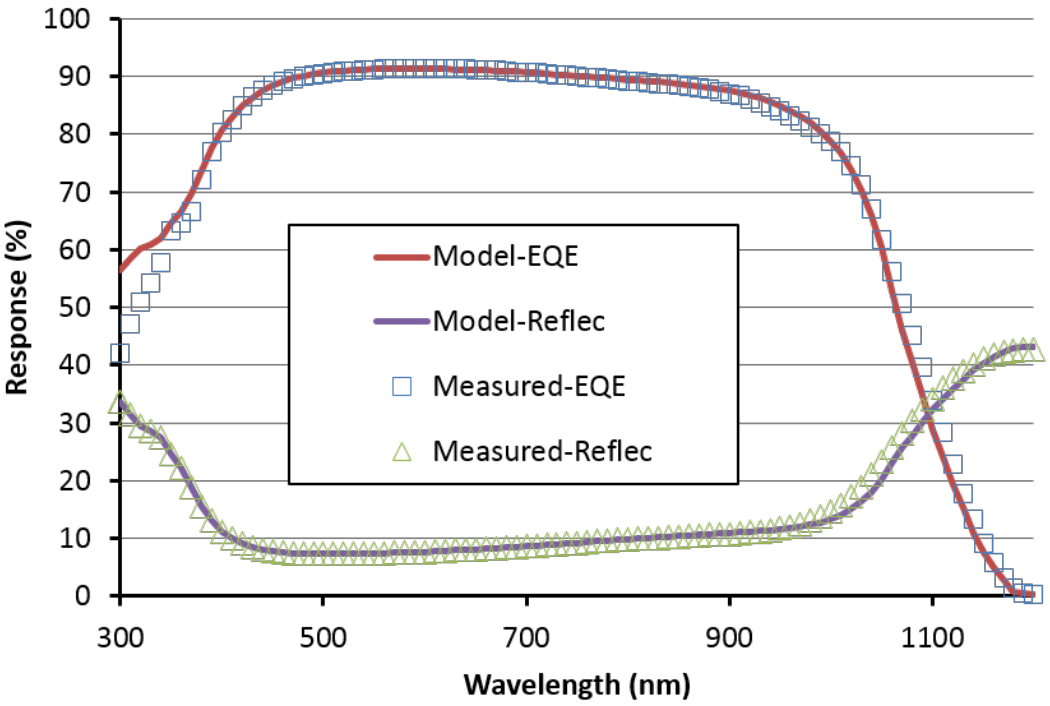
In order to quantify the impact of PSI back reflector, epi-Si cells with and without PSI were fabricated. The Light-IV, EQE and reflectance measurements are shown in Figure 40 for both types of EpiWE Si cells. LIV data shows that $J_{sc}$ improved by 2.2 mA/cm$^2$, from 34.5 to 36.7 mA/cm$^2$, due to the PSI reflector. Cell efficiency is improved by 0.5%, from 16.8 to 17.3% due to the presence of PSI reflector. This is also supported by the reflectance measurement which showed about 30% higher escape




| ID | Voc (mV) | Jsc (mA/cm$^2$) | FF (%) | Eff. (%) | Rs (Ω-cm$^2$) | Rsh (Ω-cm$^2$) |
|---|---|---|---|---|---|---|
| w/ PSI | 629 | 36.7 | 74.7 | 17.3 | 0.66 | 2350 |
| w/o PSI | 634 | 34.5 | 76.7 | 16.8 | 0.68 | 1110 |

**Figure 40:** The measured light-IV, EQE and reflectance data of EpiWE Si Cells with and without PSI back reflector.

reflectance for the wavelength exceeding 1100 nm. Note that the $R_s$ was essentially the same for the two EpiWE cells with and without PSI layer. This indicates that the designed and fabricated PSI did not introduce any appreciable resistance in the finished device, which is consistent with [53]. The 17.3% efficiency achieved in this study is among the best reported efficiency at the time for large area 90 $\mu$m epi-Si cell using EpiWE structure in combination with screen-printed contacts.




| ID | Voc (mV) | Jsc (mA/cm$^2$) | FF (%) | Eff (%) |
|---|---|---|---|---|
| Model | 628 | 36.7 | 75.5 | 17.4 |
| Measured | 629 | 36.7 | 74.7 | 17.3 |

**Figure 41:** The measured and model light-IV, EQE and reflectance data. The PC1D parameters are listed in Table 10, column w/ PSI.

PC1D modeling was performed on the screen-printed large-area EpiWE cell with PSI back reflector to understand its performance and extract the important cell parameters quantitatively [100]. A very good match was found between the modeled and measured LIV, EQE and reflectance data, as shown in Figure 41. The important

**Table 10:** The important PC1D parameters for the fabricated EpiWE cell with and without PSI back reflector

| PC1D Parameter | w/ PSI | w/o PSI |
|---|---|---|
| Thickness ($\mu$m) | 85 | 85 |
| Reflectance | Measured | Measured |
| $^1R_f$ (%) | 92 | 92 |
| $^2R_b$ (%) | 88 | 0 |
| Resistivity ($\Omega$-cm) | 2.8 | 2.8 |
| Emitter sheet ($\Omega$/sq) | 80.4 | 57.5 |
| Emitter profile | SRP-Data | SRP-Data |
| Lifetime ($\mu$s) | 100 | 100 |
| $FSRV$ (cm/s) | $3\times10^4$ | $3.5\times10^4$ |
| $BSRV$ (cm/s) | 90 | 90 |
| $J_{o2}$ (nA/cm$^2$) | 50 | 16 |
| $R_s$ ($\Omega$-cm$^2$) | 0.7 | 0.7 |
| $R_{sh}$ ($\Omega$-cm$^2$) | 2350 | 1200 |

$^1R_f$: front internal reflectance. $^2R_b$: back internal reflectance.

extracted PC1D parameters are listed in Table 10 (same analysis was also performed on the epi-Si cell without PSI as listed in Table 10 for comparison). $BSRV$ was extracted to be 90 cm/s at the p-p$^+$ interface (Figure 39 (b)) by matching the measured $V_{oc}$ and long wavelength EQE. $R_b$ at the p-p$^+$ interface was extracted to be 88% by fitting the measured and simulated escape reflectance. $R_b$ could be higher at the p$^+$-PSI interface because the BSF and free carrier absorption were not included in the PC1D calculation of the escape reflectance at the p-p$^+$ interface. Although the front cell processing is similar, the $BSRV$ and $R_b$ values of the EpiWE cell are superior to the standard industrial full Al-BSF Si solar cells, where $BSRV$ is usually $\geq$200 cm/s and $R_b$ is $\sim$65% [16]. However, the epi-Si cell efficiency is still somewhat lower than the industrial full Al-BSF cells (18-19%) because of the slightly inferior lifetime and smaller thickness.

### 6.3.2 PC1D Modeling of Si cells with Different Active Epi-Si Layer Thickness

After matching the 17.3% cell by PC1D, the modeling was extended to calculate the cell efficiency with different active epi-Si thickness by changing the thickness only while keeping all other parameters the same (Table 10). The effectiveness of the

light trapping model in PC1D for cell thickness in the range of 25 to 250 $\mu$m had been demonstrated in [94]. Our modeling results of efficiency as a function of epi-Si thickness is plotted in Figure 42, which shows that the cell efficiency drops very little with thinner epi-Si layer in this device because of the good light trapping provided by PSI formed in this study. Based on the model calculations, efficiencies of ~16.7% and ~15.7% could be attained if the cell thickness is reduced to 30 and 10 $\mu$m, respectively. EpiWE cells made by other groups in the literature (Table 1) are also plotted in Figure 42 for comparison. Our experimental and modeled cell efficiencies in Figure 42 are superior to most screen-printed EpiWE cells (blue dots) and compare very well with the other EpiWE cells which used more expensive cell technology, such

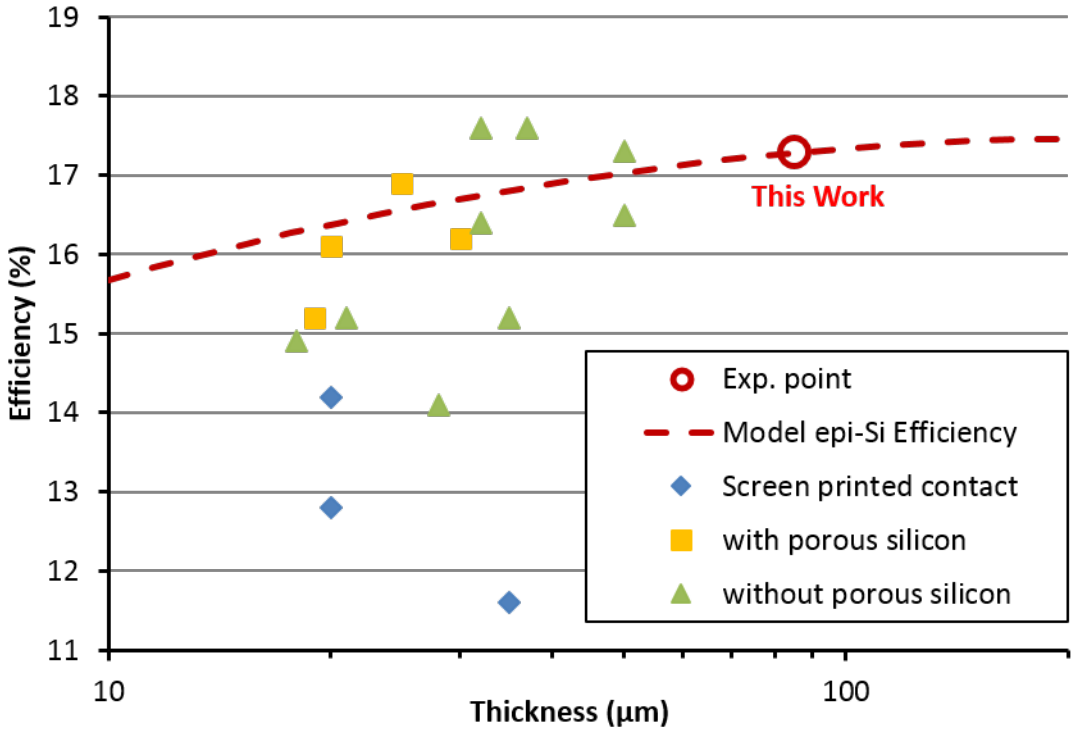



**Figure 42:** The efficiency vs epi-Si layer thickness curve of measured and model. The model curve represents the model efficiency from the experimental point with only change in thickness with key PC1D model parameters listed in Table 10. Epi-Si cell efficiency along with its thickness made by other groups (Table 1) is plotted here for comparison. Cells with higher efficiency from other groups are mainly because of photolithography contacts, inverted pyramid texture and better emitter.

as photolithography, inverted pyramid texture and better emitter.

## *6.4 Summary*

In this task, the study and optimization of PSI back reflector for thin epi-Si cells are shown. The refractive index and thickness requirements for a good PSI back reflector were established. PSI layer was formed by anodization using the model guidelines. Scattering factor at the epi-Si PSI interface was measured to be ∼99% in the long wavelength exceeding 1150 nm. Large area, screen-printed EpiWE cells with PSI back reflector were fabricated with 17.3% of efficiency. Little or no $R_s$ contribution by PSI layer was observed in the finished devices. PC1D model is used to obtain a good match between the calculated and measured LIV, EQE and Reflectance data which gives $BSRV$ and $R_b$ values of 90 cm/s and 88%, respectively. These values are superior to the standard industrial full Al-BSF Si solar cells even though the cell fabrication processes was essentially the same. The PC1D model also showed very little drop in cell efficiency for thinner active epi-Si because of the good PSI back reflector. Model shows that efficiencies of ∼16.7% and ∼15.7% could be achieved if the cell thickness is reduced to 30 and 10 $\mu$m, respectively. These results show the compatibility of PSI in Si cell processing and the promise of EpiWE Si solar cells.

# CHAPTER VII

# TASK 3: DEVELOPMENT OF SCREEN-PRINTED THIN EPI-SI SOLAR CELL USING POROUS SI LAYER TRANSFER PROCESS

In this chapter, an epi-Si based technology from epi-grown wafer to module is demonstrated, which can greatly reduce Kerf loss and give high efficiency. This concept involves forming [1]Porous Si (PSI) layer on a reusable Si substrate to not only grow but also transfer thin epi-Si active layer to a glass/EVA structure, which serves as part of the front side of the PV module and allows handling of thin epi-Si layer to finish the back side of the cell without breakage. This reduces cost because, in addition to the use of Kerfless thin epi-Si wafer, the substrate is reused for the growth of several subsequent thin epi-Si layers after removing the PSI layer on top of the substrate. Process yield was improved by a sealed edge wafer structure and texturing process optimization. Low temperature laser fired local Al contacts were developed after the lift off and layer transfer to achieve good back contact on in-situ grown full area boron doped epi-Si back surface field (BSF). Finally, material lifetime was optimized to achieve 17.2% cell efficiency on thin (90 $\mu$m), 156 cm$^2$ large epitaxially grown layer transferred Si wafers with screen-printed contacts under tabs and EVA/glass. This is equivalent to ~18.0% uncapsulated cell tested in air, assuming ~5% encapsulated loss due to reflectance and resistive loss in a module configuration. PC1D device model was used to extract the important solar cell parameters quantitatively. $BSRV$ (back surface recombination velocity) and $R_b$ (back internal reflectance) were extracted as

[1]In the case of EpiWE structure in Chapter VI (Task 2), the Porous Si (PSI) layer between the substrate and epi-Si was an integral part of cell structure to serve as a back reflector.

150 cm/s and 87%, respectively. Finally, epi-Si semi-module cells were fabricated with 15.6-17.2% efficiency under EVA/glass using 40-90 $\mu$m thick epi layers. This is the first time large area thin epi-Si cells have been fabricated using layer transfer technology in combination with industrial type screen-printed front contacts.

## *7.1 Process Flow for Screen-printed Thin Epi-Si Cells using PSI Layer Transfer Process*

This cell fabrication process (Figure 43) can be divided into four parts: wafer preparation, front cell process, semi-module process, back cell process and module assembly.

### 7.1.1 Wafer Preparation

A PSI layer was first formed by electrochemical etching of a heavily boron doped ($\sim$0.01 $\Omega$-cm) p-type $\sim$750 $\mu$m thick mono-Si substrate (Figure 43 a). The substrate with PSI layer on the top surface was then subjected to a high temperature anneal to form the Si seed layer. The epitaxial Si layer was grown on this Si seed layer at the rate of $\sim$4 $\mu$m/min. A $p^+$ layer was first grown to form a built-in BSF followed by 40-90 $\mu$m 1-3 $\Omega$-cm B-doped epi-Si layer, as shown in Figure 43 (b).

### 7.1.2 Front Cell Processing

The epi-Si wafers were processed into cells by: (a) anisotropic texturing in KOH based solution to attain 4-6 $\mu$m random pyramids, (b) $POCl_3$ diffusion to obtain 60-85 $\Omega$/sq emitter on the front textured surface, (c) phosphosilicate glass (PSG) removal, (d) deposition of PECVD $SiN_x$ antireflection coating on the $n^+$-emitter, (e) screen printing front Ag grid, and (f) front contact firing in a commercial belt furnace. Figure 43 (c) shows the wafer structure after the above processing. This process sequence is also shown in Figure 43.

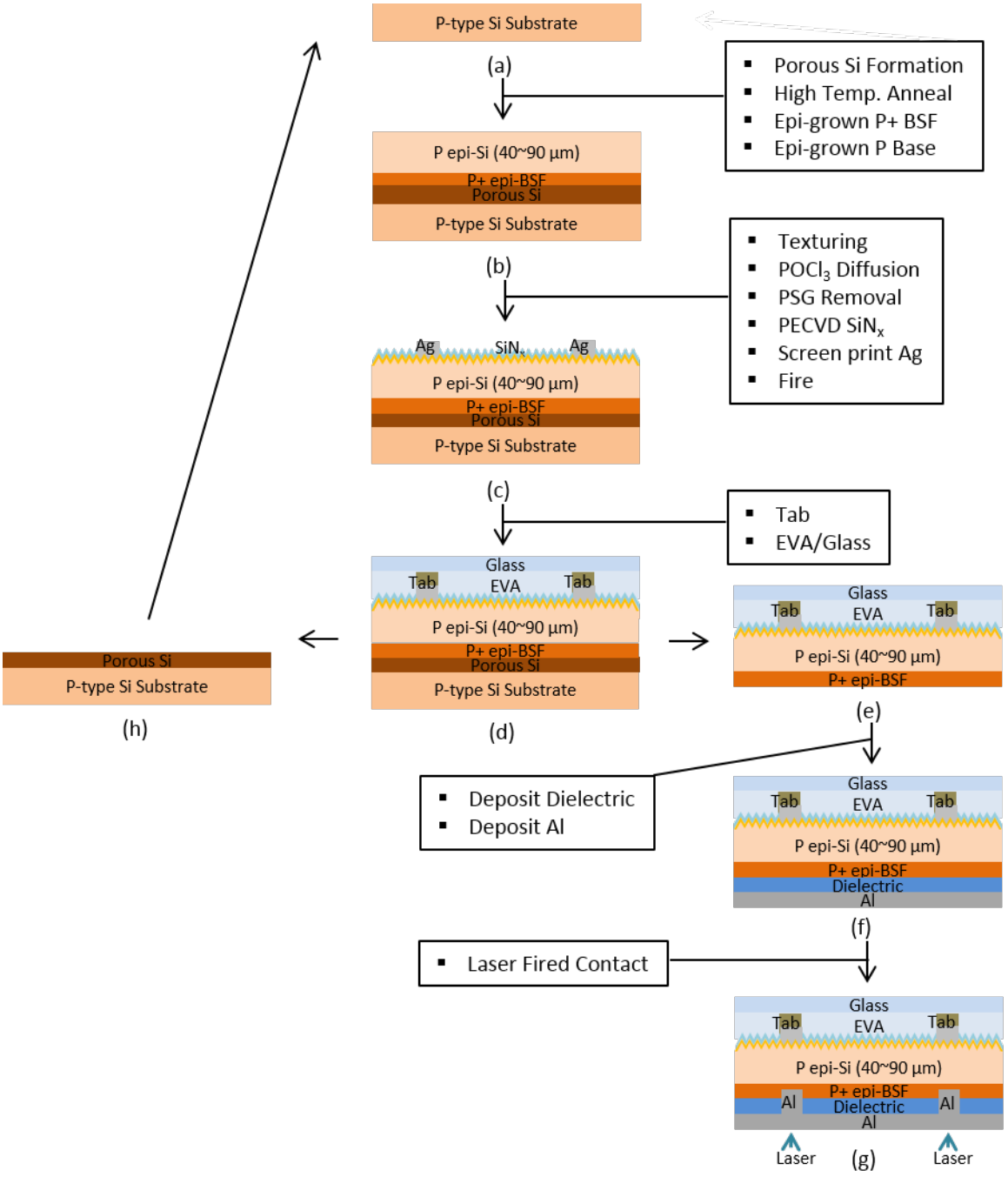



**Figure 43:** Epi-Si cell process flow: (a) The starting substrate or re-usable substrate after cleaning. (b) Epitaxially grown Si on porous Si and substrate. (c) The cell structure after front cell processing. Textured surface, emitter, $SiN_x$ and screen-printed contact finished. (d) The cell structure after tabbing and lamination. (e) The device layer after exfoliation. (f) The device layer after back dielectric and Al deposition. (g) Laser fired contact. The cell is ready to measure. (h) The substrate after exfoliation.

### 7.1.3 Semi-module Processes

The front side of the processed cell was laminated with standard tabbing of the front grid followed by EVA/glass encapsulation on the front side of the cell, as shown in Figure 43 (d). Following that, the epi-Si layer was exfoliated from the substrate with the help of PSI as shown in Figure 43 (e) and (h). The thin epi-Si (Figure 43 e) wafer is now supported and protected by the EVA/glass and the separated substrate (Figure 43 h) is good for reuse (Figure 43 a) to reduce Kerf loss. The exfoliated epi-Si sample is now ready for low temperature back processing.

### 7.1.4 Back Cell Processing

The back side processing involved a low temperature deposition of ~20 nm thick $SiO_2$ and Al to form a back reflector as shown in Figure 43 (f). Finally, localized laser fired Al ohmic contacts were formed to the boron doped BSF using a UV laser (Figure 43 g) to punch through the dielectric and drive Al to contact Si. Note that at this point the finished cell is like a semi-module with EVA/glass layers on top side (Figure

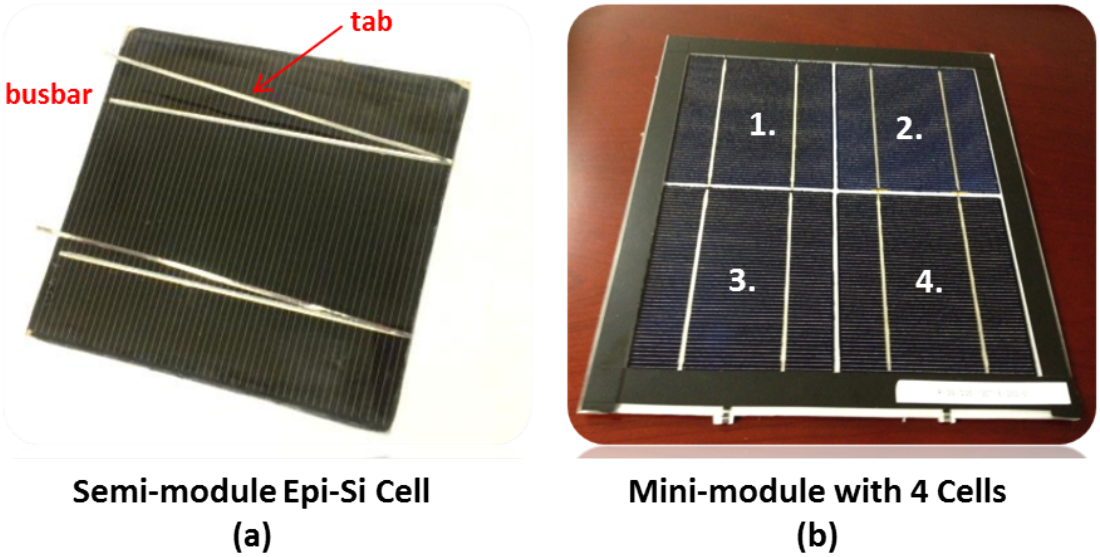



**Figure 44:** Picture of a finished semi-module cell (a) and a mini-module made of 4 cells (b).

43 g and Figure 44 a). All the cell efficiency numbers reported for this technology were measured on this semi-module structure which results in slightly lower efficiency compared to the corresponding large area screen-printed Si cells tested in air. This is because EVA/glass encapsulation and tabbing can often amount to as much as ~5% relatively efficiency loss due to reflection and resistance.

### 7.1.5 Module Assembly

The module fabrication process sequence is similar to conventional Si cells. A mini-module containing four cells is shown in Figure 44 (b) where top of one cell is connected to the back of the adjacent cell by tabbed ribbon.

## *7.2 Yield Improvement and Texturing Optimization*

In the beginning of the task, a key challenge was to improve the process yield. A

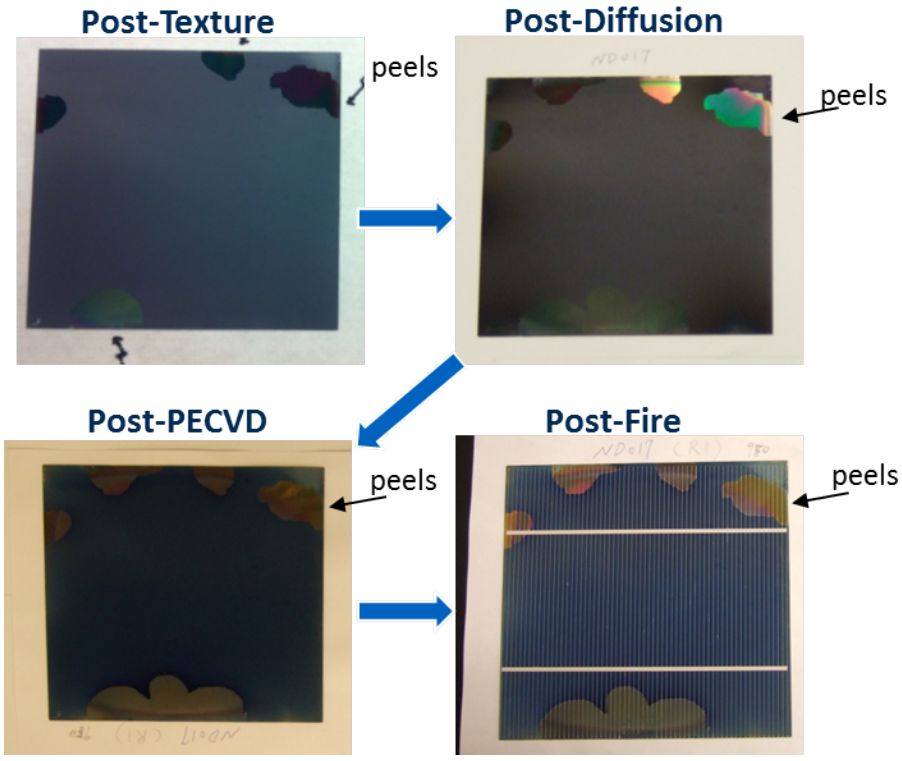
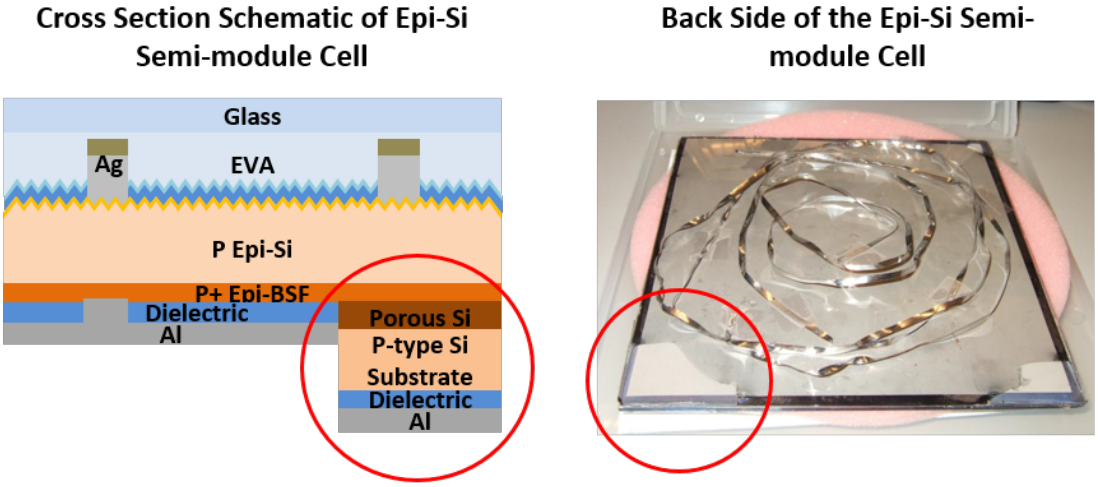



**Figure 45:** Picture of peeled thin active epi-Si layer on top of the PSI and substrate during the front cell processing. The peeling increases through out the process.

lot of effort was made to optimize the PSI mechanical strength, which is controlled by the PSI porosity and the anodizing current as discussed in Section 6.1.3. If the strength is inadequate, the thin epi-Si active layers peels off during the front cell processing (especially during the texturing process), as shown in Figure 45. No cells can be finished on these kind of wafers. However, if the PSI layer is too strong, the thin epi-Si active layers cannot be exfoliated/separated completely, as shown in Figure 46. Some fraction of the substrate remained at the corners of the exfoliated cell. The substrate was then broken and could not be reused. The first semi-module epi-Si solar cell fabricated in this study had an efficiency of 10.7% with incomplete exfoliation.

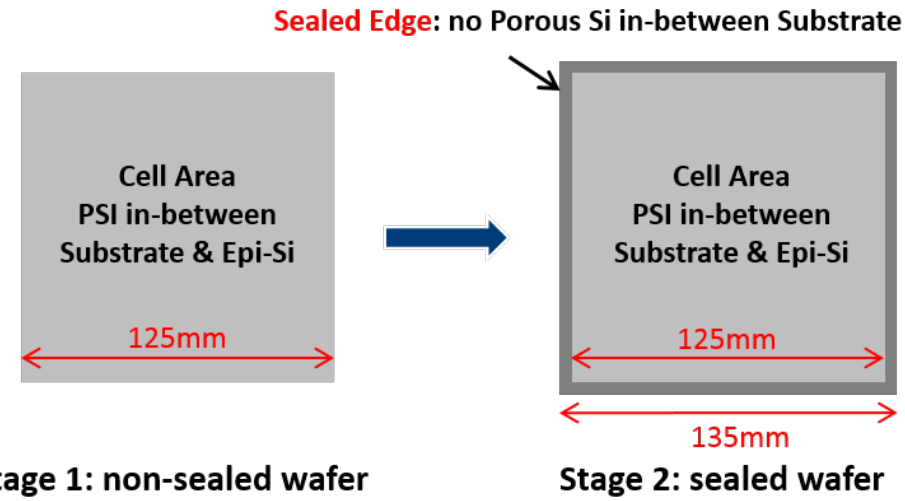



| ID | Area ($cm^2$) | $V_{oc}$ (mV) | $J_{sc}$ ($mA/cm^2$) | $FF$ (%) | Efficiency (%) | $R_s$ ($\Omega$-$cm^2$) | $R_{sh}$ ($\Omega$-$cm^2$) |
|---|---|---|---|---|---|---|---|
| First Cell | 156 | 563 | 27.6 | 68.8 | 10.7 | 2.23 | 294 |

**Figure 46:** Picture of the non-fully exfoliated epi-Si semi-module cell and the light IV data of the first cell.

The problem was solved by implementing a "sealed edge" (thin active epi-Si layer/ substrate) on the side of the epi-Si wafer structure (thin active epi-Si layer/ PSI/ substrate), as shown in stage 2 of Figure 47. In stage 1 (Figure 47), PSI layer was in-between the thin active epi-Si layer and the substrate with full substrate area, resulting in very low yield. The sealed edge was implemented in stage 2. There was

no PSI layer in-between the substrate and the thin epi-Si active layer under the sealed edge area. Therefore, the exfoliated cell area was smaller than the substrate. The non-exfoliated sealed area protected the wafer structure better during the processes. A laser scribing process was used at the cell area edge before the thin epi-Si layer could be separated from the substrate by a mechanical force. As shown in Figure 47, much better yield of 93% was achieved by the sealed edge wafer structures.




| Stage | # of wafers as started | # of wafers after texturing | Yield | cell size | edge |
|---|---|---|---|---|---|
| Stage 1 | 43 | 25 | 58% | 125*125mm | non-sealed |
| Stage 2 | 133 | 124 | 93% | 125*125mm | sealed |

**Figure 47:** Texturing process yield improvement with sealed edge wafer structure compared to non-sealed wafer.

In order to further improve the yield during texturing process, one should have as little Si consumption as possible. Too much Si consumption during texturing damages the Si edge between the sealed and cell area, resulting in thin epi-Si layer peel off. However, it was difficult to get low reflectance with too little Si consumption in the normal KOH based texturing solution. Different additives to texturing solution were tested to get low reflectance and reduced Si consumption at the same time. Figure 48 shows the relationship between Si consumption, reflectance and texturing time

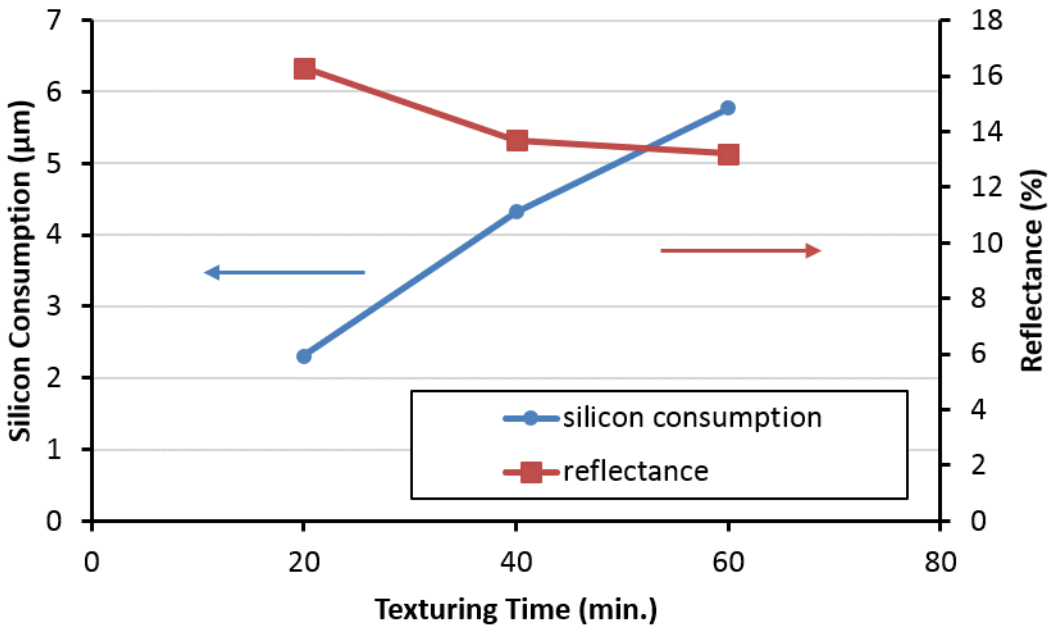



**Figure 48:** Relationship between the Si consumption, reflectance and texturing time with the right commercial texturing additive.

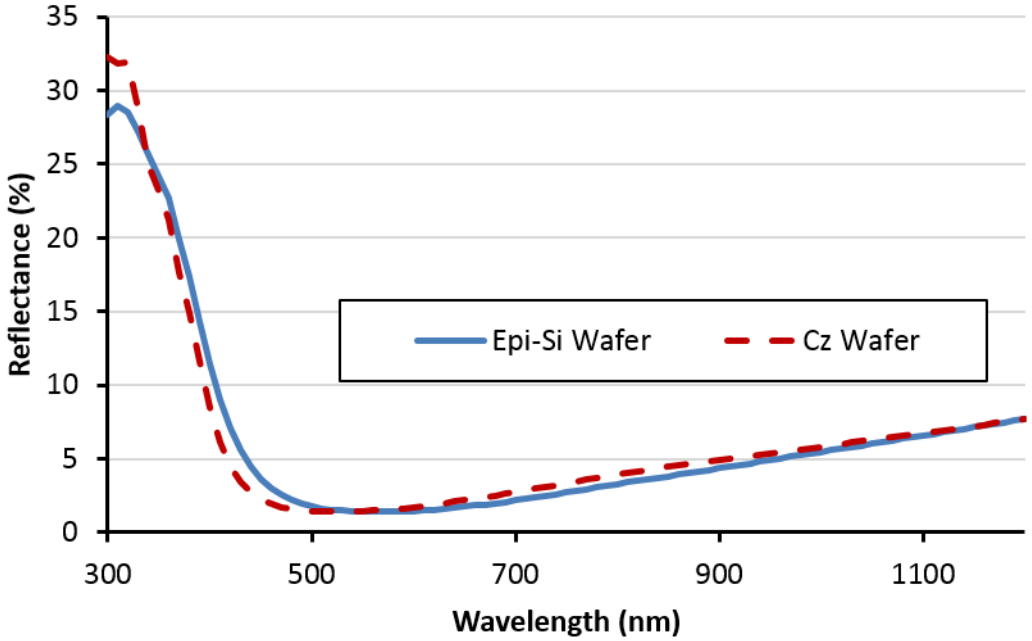



**Figure 49:** Reflectance comparison between the epi-Si wafers by adding texturing additive ($\sim$6 $\mu$m Si consumption) and standard Cz wafer texturing process ($\sim$15 $\mu$m Si consumption)

using the right additive to our KOH based texturing solution. Good reflectance was achieved with only ∼6 $\mu$m Si consumption compared to ∼15 $\mu$m in the normal texturing process.

Figure 49 shows the reflectance comparison between the epi-Si wafers and commercial Cz wafers after texturing and anti-reflection coating. These textured Cz wafers also gave >19% efficient solar cells, which is comparable to our standard full Al-BSF screen-printed baseline process. Thus, our modified texturing process with less Si consumption does not introduce any efficiency loss compared to the commercial full Al-BSF Si solar cells.

## *7.3 Laser Fired Contact*

In the beginning of this task, the dielectric back was first opened with laser followed by Al deposition to form the mirror and local contacts to $p^+$ BSF. However, this approach needed ∼400 °C anneal [101] to achieve good ohmic contact. This process was not compatible with the exfoliated semi-finished semi-module cell (Figure 43 d) with tab/EVA/glass on front because the tab and EVA cannot withstand >230 °C temperature. This led to the development of laser fired contact (LFC) process first proposed by investigators at Fraunhofer Institute [71, 102, 103], which involves depositing the Al on the dielectric layer first and then locally forming the contacts by laser firing Al through the dielectric. Here, Al and Si are locally heated and melted by laser to form good contact. No additional anneal is required. In this study, the back contact spacing was kept to be ∼500 $\mu$m and the contact diameter was about ∼120 $\mu$m wide.

A q-switched solid state ultraviolet nanosecond laser in TEM00-mode with 355 nm wavelength was used in this research. The laser pulse energy was gradually increased from 0% to 100% (150 $\mu$J) to optimize the laser power as shown in Figure 50 and 51. Figure 52 shows optical microscope images of local contacts as a function

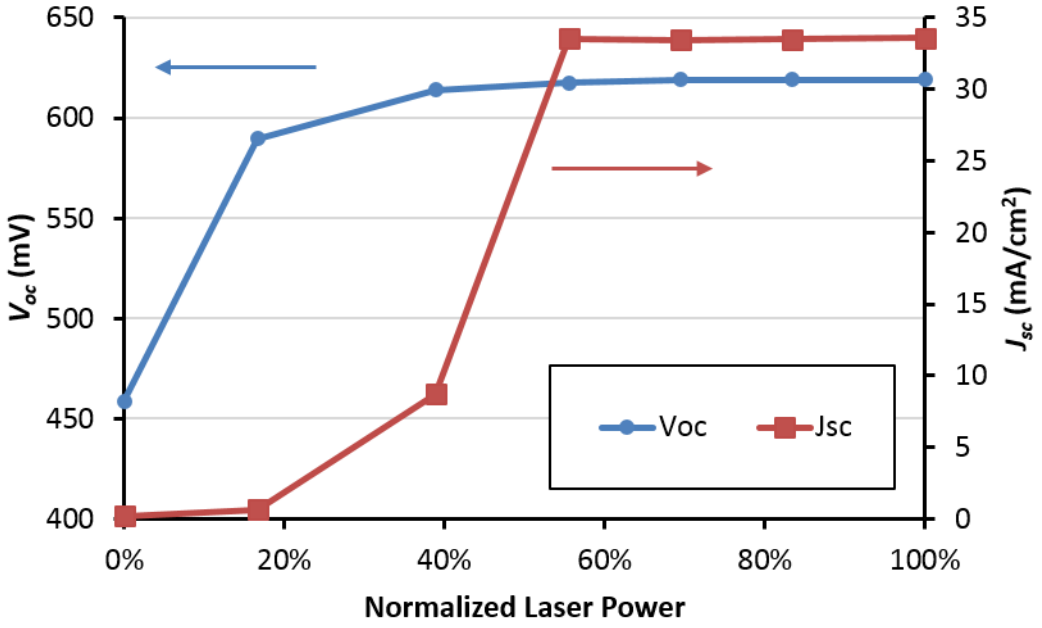



**Figure 50:** The laser power optimization of laser fired contact. $V_{oc}$ and $J_{sc}$ increase as laser power increases.

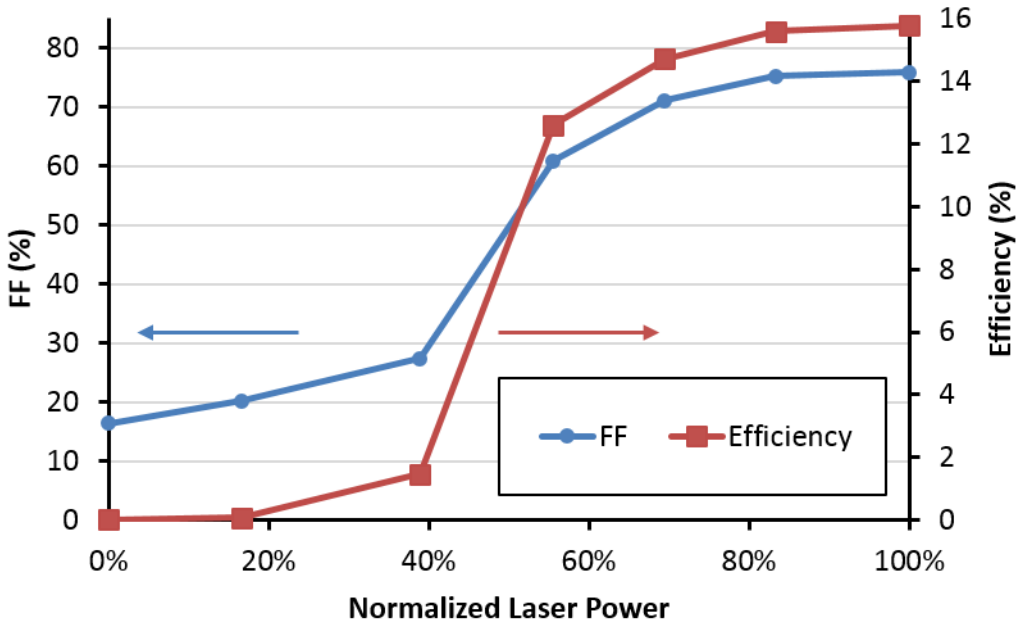



**Figure 51:** The laser power optimization of laser fired contact. $FF$, and $\eta$ increase as laser power increases.

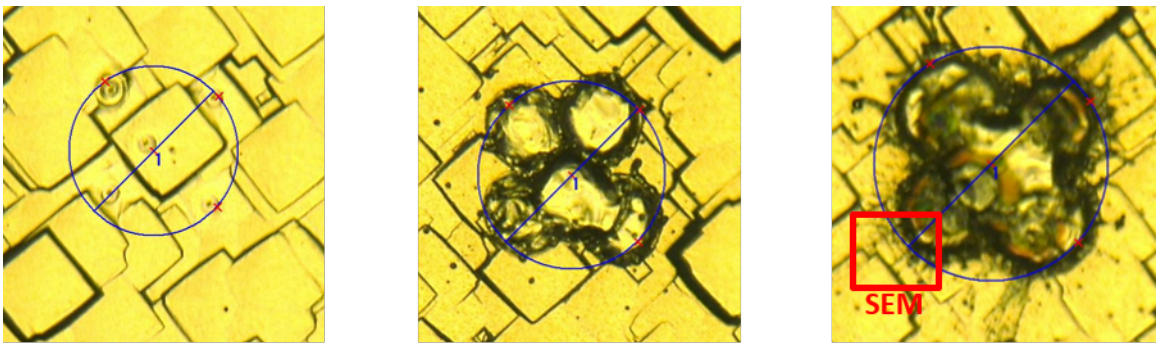



**Figure 52:** Optical microscope images of laser irradiated regions for laser fired contact with different laser power of 17%, 56%, and 100%. The SEM picture for 100% laser power is shown in Figure 53.

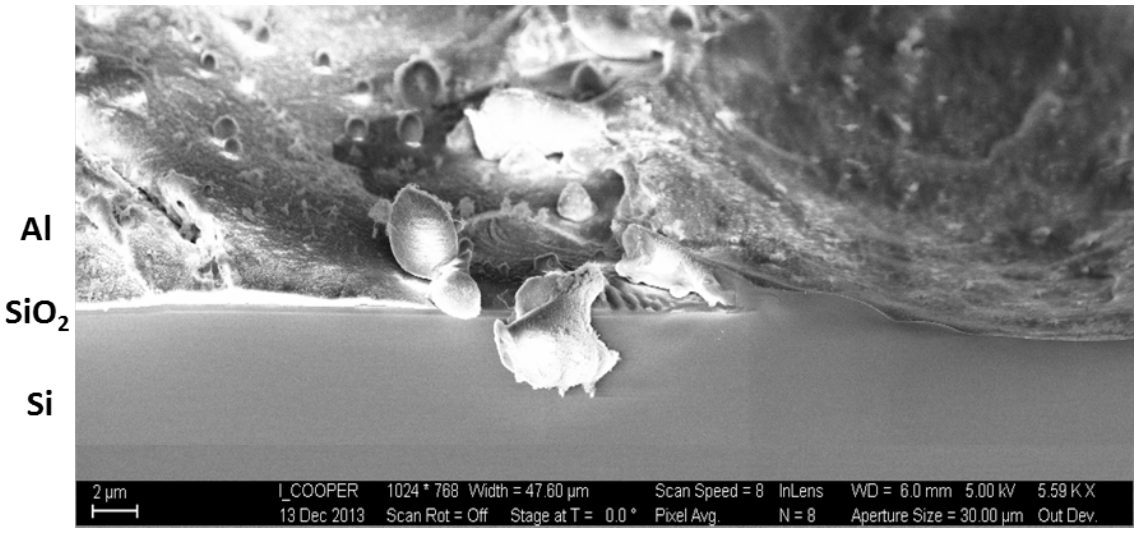



**Figure 53:** The SEM of the cross section of the 100% power laser fired contact.

of laser power. It was found that all the light IV parameters including $V_{oc}$, $J_{sc}$, and $FF$ improved initially and then saturated at higher laser power. $V_{oc}$, $J_{sc}$, $FF$, and $\eta$ increased to 619 mV, 33.6 mA/cm$^2$, 75.9% and 15.8% at 100% laser power, respectively, compared to $V_{oc}$ of 614 mV, $J_{sc}$ of 8.7 mA/cm$^2$, $FF$ of 27.4% and $\eta$ of 1.5% at 40% laser power.

While little damage or melting of the Al surface was observed with 17% laser power in the irradiated area, Al surface melting/damage was clearly observed with

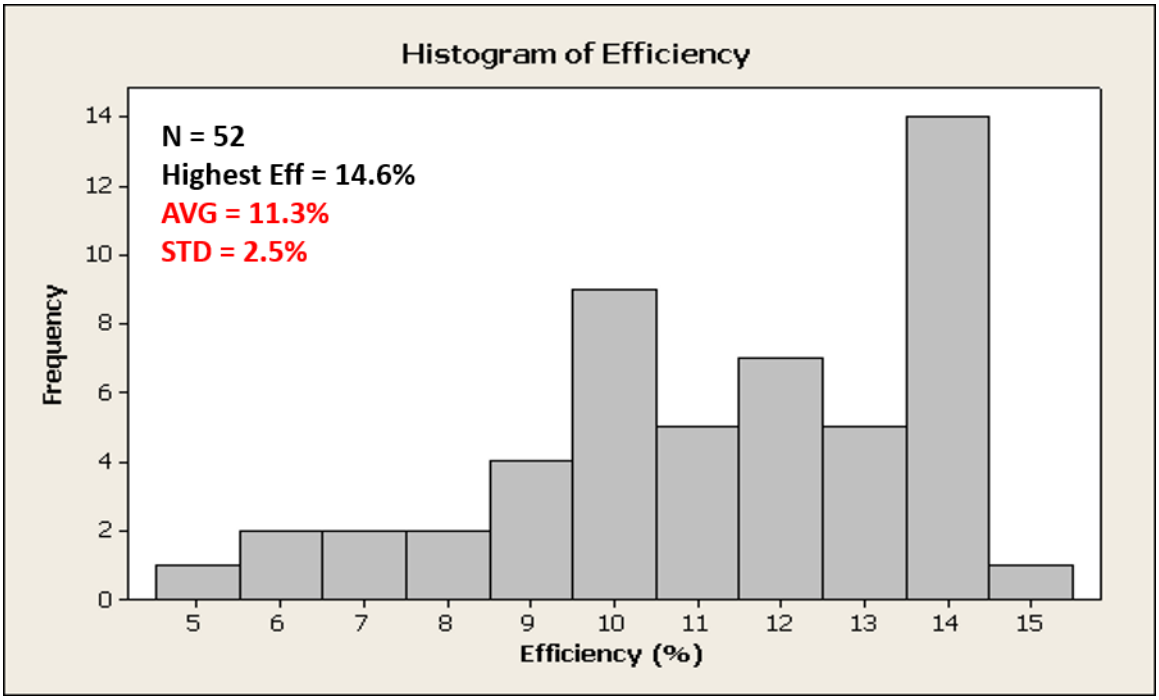



**Figure 54:** The histogram of finished cell efficiency by laser opening process.

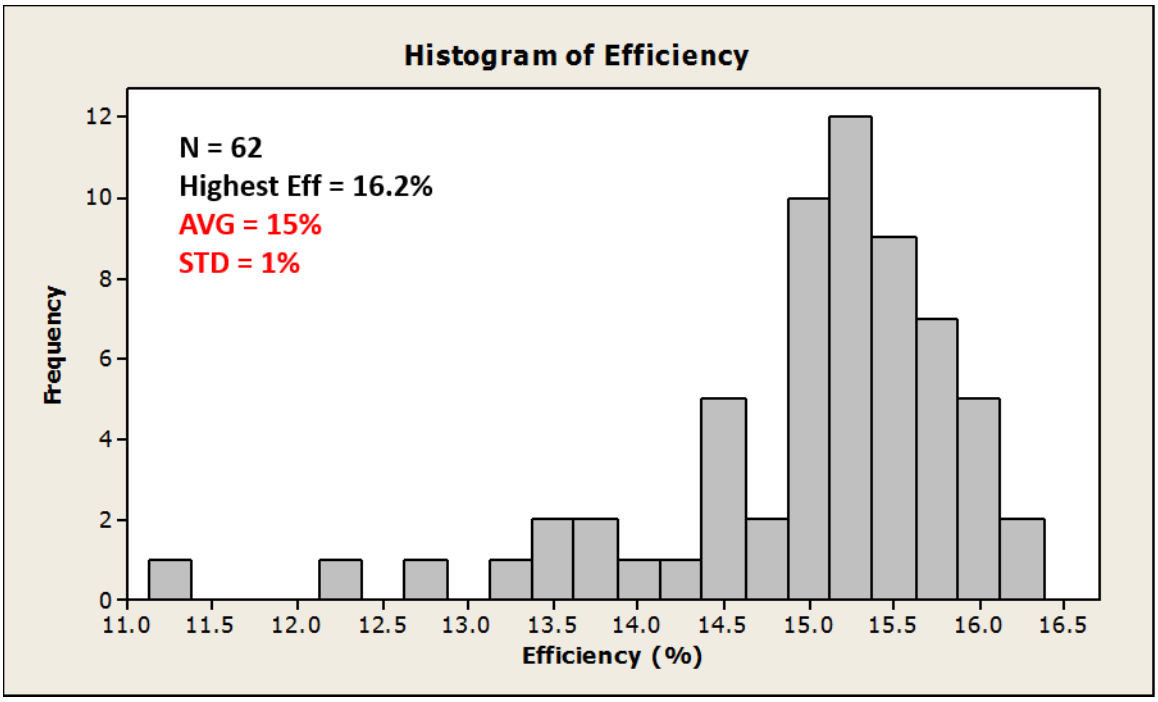



**Figure 55:** The histogram of finished cell efficiency by laser fired contact process.

100% laser power, which gave the best cell performance (Figure 51). The SEM picture (Figure 53) at the edge of the contact formed with 100%-laser-power clearly shows that $SiO_2$ layer is completely removed under the laser fired contact. This supports better $FF$ (75.9%) observed in Figure 51 for higher laser power.

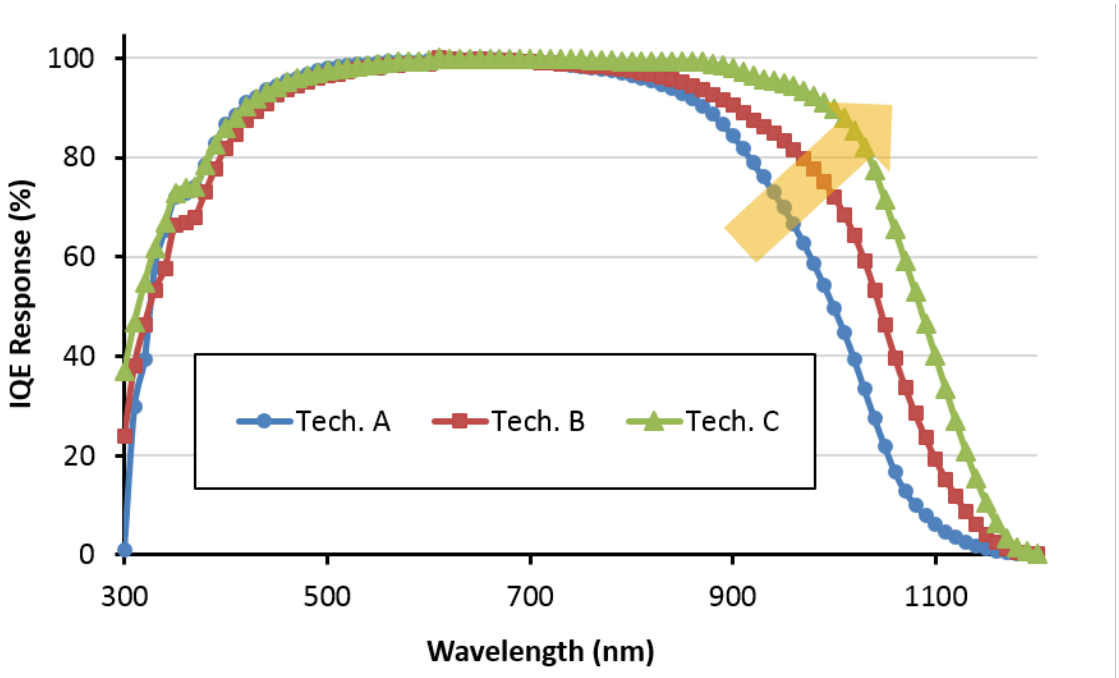
Figure 54 and 55 show the finished cell efficiency histograms for laser opening and laser fired back contact technologies, respectively. Laser fired contact process not only enhanced the average cell efficiency by 3.7%, from 11.3% to 15.0%, but also improved the standard deviation by 1.5%, from 2.5% to 1.0%. This is mainly because of the improved $FF$ as a result of lower $R_S$ or back contact resistance, as shown in Table 11.

**Table 11:** LIV comparison between the laser opening and laser fired contact processes

| Process | $V_{oc}$ (mV) | $J_{sc}$ (mA/cm$^2$) | $FF$ (%) | Efficiency (%) | $R_s$ ($\Omega$-cm$^2$) | $R_{sh}$ ($\Omega$-cm$^2$) |
|---|---|---|---|---|---|---|
| Laser Opening + anneal | 625 | 33.8 | 48-70 | 10.1-14.8 | 2-5.2 | 1150 |
| Laser Fired Contact | 626 | 33.9 | 71-76 | 15.0-16.1 | ~0.9 | 4654 |

## *7.4 Optimization of Built-in Boron BSF Design and Bulk Lifetime*

Both BSF design and bulk lifetime are the key to high efficiency thin epi-Si cells. Therefore, we fabricated and measured cells with different bulk resistivities, bulk lifetimes, and BSF profiles (Figure 56). Figure 56 shows that a 13.2% epi-Si semi-module cell was obtained on a low bulk lifetime (1 $\Omega$-cm, ~3 $\mu$s) base with heavily doped BSF ($5.5\times10^{19}$ cm$^{-3}$, 10 $\mu$m) (Tech. A). Next, the BSF doping was lowered to reduce the Auger recombination with slightly better bulk lifetime (~5 $\mu$s) material, resulting in 14.1% efficiency (Tech. B). Finally, a 17.2% epi-Si semi-module cell was achieved using ~100 $\mu$s, 2.8 $\Omega$-cm Si in combination with $5\times10^{18}$ cm$^{-3}$, 4 $\mu$m thick BSF (Tech. C). Increase in long wavelength IQE response in Figure 56 supports the




| ID | Resis. (Ω-cm) | τ (μs) | BSF | $V_{oc}$ (mV) | $J_{sc}$ (mA/cm$^2$) | FF (%) | η (%) | $R_s$ (Ω-cm$^2$) | $R_{sh}$ (Ω-cm$^2$) |
|---|---|---|---|---|---|---|---|---|---|
| Tech. A | 1 | ~3 | 5.5×10$^{19}$ cm$^{-3}$, 10 μm | 601 | 31.9 | 68.9 | 13.2 | 2.5 | 783 |
| Tech. B | 2 | ~5 | 2×10$^{19}$ cm$^{-3}$, 4 μm | 614 | 32.2 | 71.5 | 14.1 | 1.9 | 1046 |
| Tech. C | 2.8 | ~100 | 5×10$^{18}$ cm$^{-3}$, 4 μm | 623 | 35.9 | 77.0 | 17.2 | 1.0 | 6500 |

**Figure 56:** The measured light-IV and IQE data for different lifetime and BSF epi-Si cell.

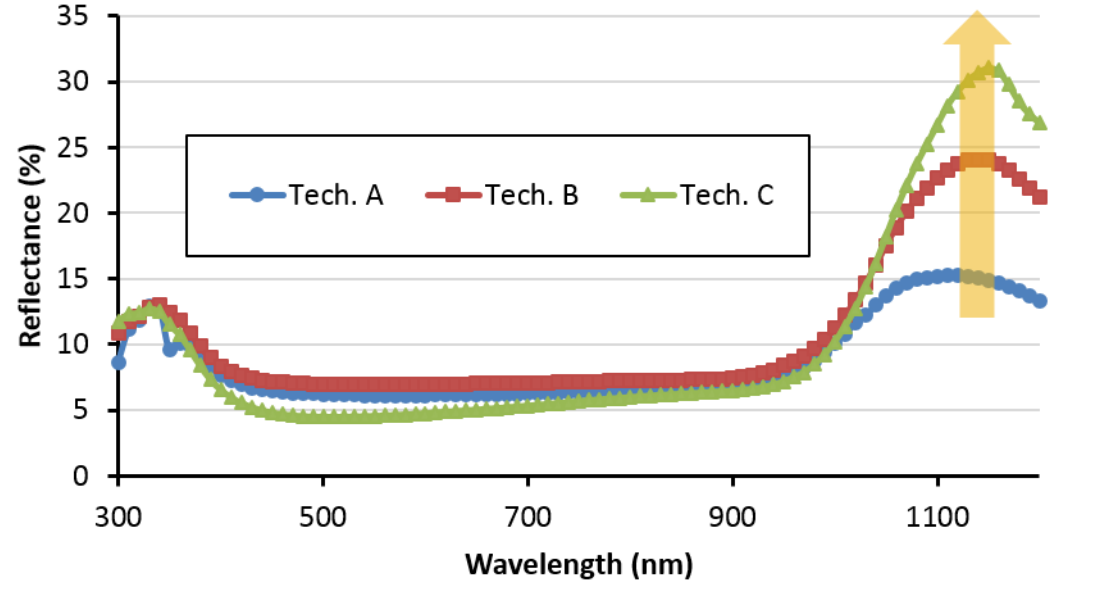
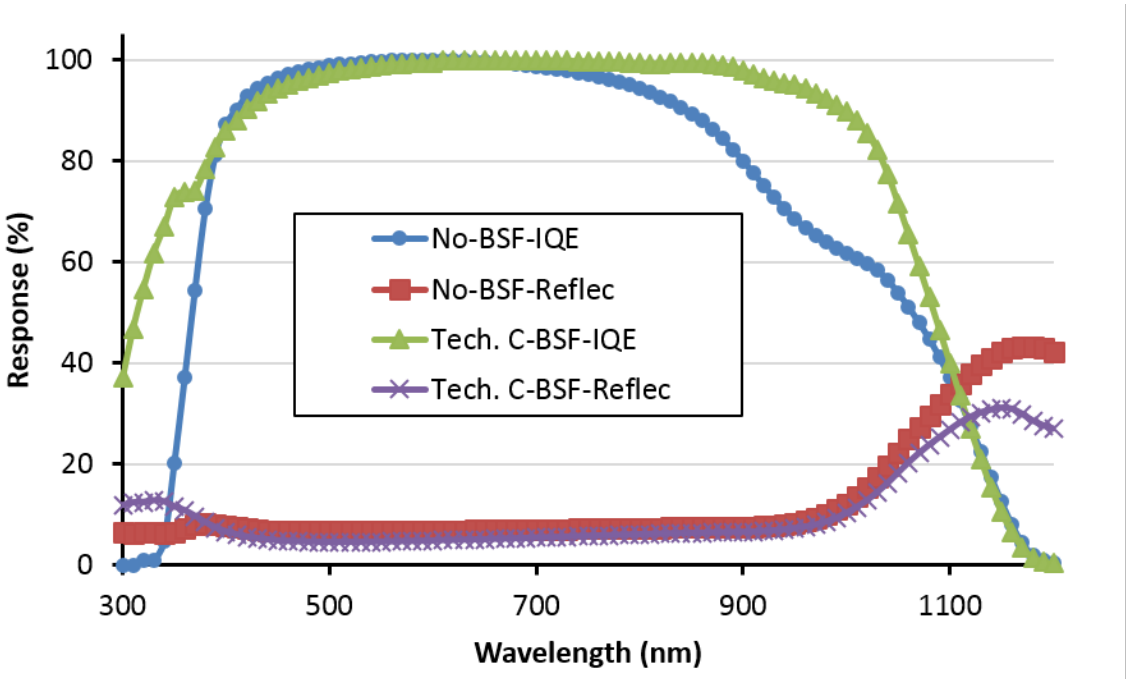



**Figure 57:** The measured reflectance data for different lifetime and BSF epi-Si cell.

importance of high bulk lifetime and BSF design for this device structure. The lighter BSF also increased the escape reflectance (>1000 nm) (Figure 57) because of reduced free carrier absorption [5]. The 17.2% epi-Si semi-module cell achieved in this study is equivalent to ~18.0% uncapsulated cell tested in air because of ~5% encapsulation loss due to tab/EVA/glass induced reflectance and resistive loss.




| ID | BSF | $V_{oc}$ (mV) | $J_{sc}$ (mA/cm$^2$) | $FF$ (%) | η (%) | $R_s$ (Ω-cm$^2$) | $R_{sh}$ (Ω-cm$^2$) |
|---|---|---|---|---|---|---|---|
| No-BSF | n/a | 562 | 32.3 | 74.2 | 13.4 | 1.4 | 5660 |
| Tech. C-BSF | 5×10$^{18}$ cm$^{-3}$, 4 µm | 623 | 35.9 | 77.0 | 17.2 | 1.0 | 6500 |

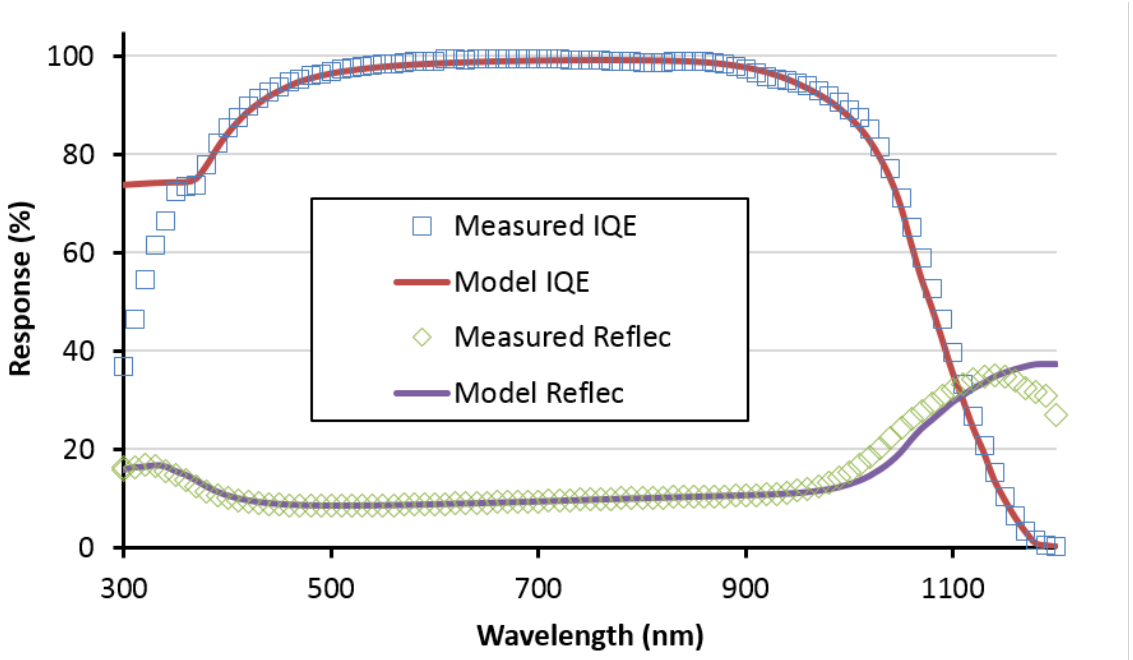
**Figure 58:** Measured IQE and Reflectance data for the with and without BSF cells. The measured data was EQE and Reflectance while IQE was calculated by IQE=EQE/(1-Reflectance).

In order to validate and quantify the effectiveness of the built-in epi-grown BSF, we fabricated cells with and without the epi-Si BSF layer. The measured light IV data in Figure 58 shows that epitaxially grown in-situ BSF accounts for 61.5 mV difference in $V_{oc}$, 3.6 mA/cm$^2$ in $J_{sc}$, and 3.8% in absolute efficiency. Figure 58 also shows the IQE and reflectance data of the semi-module epi-Si cells with and without

**Table 12:** The important PC1D parameters for the 17.2% epi-Si semi-module cell

| PC1D Parameter | Values |
|---|---|
| Thickness ($\mu$m) | 85 |
| Reflectance | Measured |
| $^1R_f$ (%) | 92 |
| $^2R_b$ (%) | 87 |
| Resistivity ($\Omega$-cm) | 2.8 |
| Emitter sheet ($\Omega$/sq) | $\sim$70 |
| Emitter profile | SRP-Data |
| Lifetime ($\mu$s) | 100 |
| $FSRV$ (cm/s) | $8\times10^4$ |
| $BSRV$ (cm/s) | 150 |
| $J_{o2}$ (nA/cm$^2$) | 23 |
| $R_s$ ($\Omega$-cm$^2$) | 1.0 |
| $R_{sh}$ ($\Omega$-cm$^2$) | 6500 |

$^1R_f$: front internal reflectance. $^2R_b$: back internal reflectance.




| ID | $V_{oc}$ (mV) | $J_{sc}$ (mA/cm$^2$) | $FF$ (%) | Efficiency (%) |
|---|---|---|---|---|
| Model | 622.4 | 36.1 | 76.1 | 17.1 |
| Measured | 623.2 | 35.9 | 77.0 | 17.2 |

**Figure 59:** The measured and model light-IV, IQE and reflectance data. The PC1D parameters are listed in Table 12

BSF. We can clearly see a huge difference in the long wavelength IQE response due to the BSF for these thin base ($\leq$90 $\mu$m) epi-Si cells. Note that the IQE measurements were done on encapsulated cells. Therefore, the IQE response in Figure 58 is very low below 400 nm due to the glass/EVA absorption. Finally, PC1D modeling was performed on the 17.2% screen-printed large-area epi-Si semi-module solar cell to extract important parameters listed in Table 12 [100]. A very good match was found between the modeled and measured light IV, IQE and reflectance data, as shown in Figure 59. Extracted values for $BSRV$ and back internal reflectance ($R_b$) were 150 cm/s and 87%, respectively, at the p-p$^+$ interface. This compares very well with the epi-Si EpiWE cells made in Task 2 (Chapter V), where the extracted $BSRV$ and $R_b$ values were 90 cm/s and 88%, respectively.

## *7.5 Epi-Si Cells with Different Bulk Thickness*

Semi-module epi-Si cells with different epi-Si thickness were fabricated using the process flow described in section 7.1. The light IV data as function of epi-Si thickness is shown in Figure 60. The best experimental semi-module cell efficiency for 40, 50, 60, 70, 80, and 90 $\mu$m thick epi-Si was 15.9%, 15.8%, 16.1%, 16.9%, 16.7%, 17.2%, respectively. This is the first time screen-printed large-area thin epi-Si solar cells under EVA/glass have been fabricated using layer transfer process.

## *7.6 Summary*

A promising epitaxial Si based technology from wafer to module is demonstrated in the task. Thin wafers were prepared at Crystal Solar Inc. on a reusable substrate with porous Si layer using epitaxially grown Si. Front side of the cells was processed using standard $POCl_3$ diffusion emitter, PECVD AR coating, screen-printed contacts, and laminated with standard EVA/glass. After exfoliation of the epi-Si layer from the substrate using the PSI layer transfer process, rear side of the cell was finished by dielectric/metal deposition and laser fired contacts. A sealed edge wafer structure

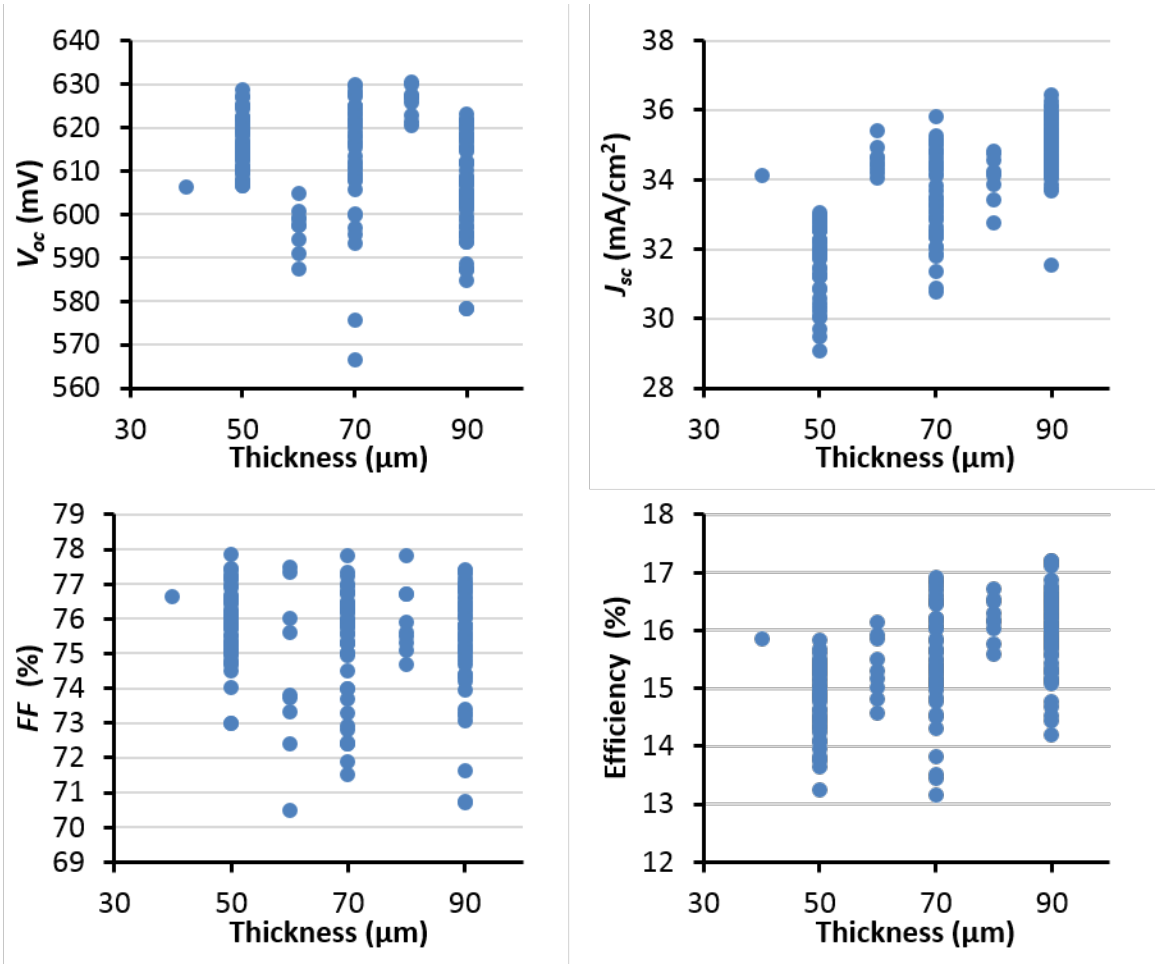



**Figure 60:** Measured light IV data for different thickness epi-Si cells made in UCEP, Georgia Tech. Total 175 cells are shown in the figure.

and texturing optimization was studied and developed to improve the over all process yield. Low temperature laser fired contact process was developed and optimized to make the local back contact to the $p^+$ BSF. A 17.2% efficiency was achieved with the EVA/glass encapsulation, which corresponds to ~18.0% cell efficiency without encapsulation. $BSRV$ and $R_b$ values of 150 cm/s and 87% were extracted by PC1D device modeling. Several 40-90 $\mu$m thick epi-Si semi-module cells were fabricated with 15.6-17.2% efficiency with EVA/glass encapsulation. This is the first demonstration of large area thin epi-Si cell fabrication using layer transfer technology in combination with industrial screen-printed technology.

# CHAPTER VIII

# TASK 4: DEVELOPMENT OF SCREEN-PRINTED EPI-SI SOLAR CELL ON FREE-STANDING EPI-SI KERFLESS WAFER

In Task 4, high efficiency screen-printed cells were fabricated on p-type and n-type stand alone epi-Si wafers with thickness in the range of 120-180 $\mu$m. Close to 20% efficiency is demonstrated using industrial type PERC and PERT processes on p-type and n-type epi-Si wafers, respectively. These efficiencies were slightly lower or comparable to the cells made on commercial grade Cz wafers using the identical process. In addition, p-type boron doped epi-Si cells showed no light induced degradation in efficiency while Cz cells showed significant efficiency degradation. This demonstrates that epi-Si technology is very attractive for the PV industry since epi-Si wafers can be significantly cheaper than the traditional Cz wafers due to the elimination of producing Poly-Si feedstock, crystal growth and Kerf loss.

## *8.1 Fabrication and Comparison of P-type PERC cells on Epi-Si and Commercial Grade Cz Si wafers*

To compare the material quality of epi-Si and traditional Cz Si wafers, cells were fabricated simultaneously on two different epi-Si wafers (Epi-p1: 2.4 Ω-cm/150 $\mu$m thick and Epi-p2: 3.7 Ω-cm/180 $\mu$m thick) as well as commercial grade Cz wafers (2.2 Ω-cm/170 $\mu$m thick). A screen-printed p-type PERC process [16] was developed and used which involved (a) random pyramid anisotropic texturing in a KOH based solution, (b) single side planarization in 9% KOH solution at 80 °C for 900 sec., (c) phosphorous ion implantation on the front with $2.8\times10^{15}$ P/cm$^2$ and energy 10

keV, (d) standard RCA clean, (e) implant anneal and thermal oxide passivation at 855°C with 20 minutes oxidation and 10 minutes nitrogen anneal, (f) PECVD $SiN_x$ deposition on the front (450 sec.) and on the back (2000 sec.), (g) local laser opening of the back dielectric with 1 mm spacing line pattern (∼75 $\mu$m opening) and laser pulse energy of >150 $\mu$J, (h) BOE dip for 30 sec. (or 2% HF for 60 sec.) (i) screen printing of Ag grid using DuPont 17S silver paste on the front (89 lines and 3 busbars) and Monocrystal EFX-37 Al paste on the back, and (j) front and back contact firing in a belt furnace. The finished cell structure is shown in Figure 61.

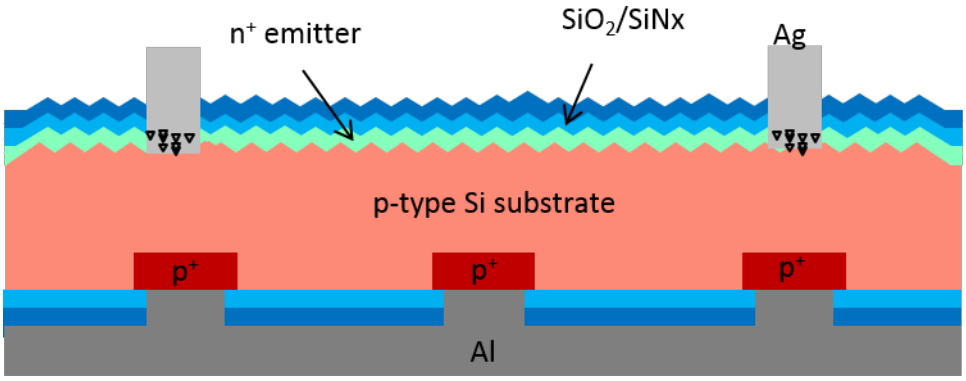



**Figure 61:** The Schematic cross-section of screen-printed p-type PERC cell.

**Table 13:** The measured LIV data for p-type PERC cell using Cz and epi-Si material

| Device ID | Material | Resis. (Ω-cm) | Thick. ($\mu$m) | $V_{oc}$ (mV) | $J_{sc}$ (mA /cm$^2$) | $FF$ (%) | Eff. (%) | $R_s$ (Ω-cm$^2$) | Rsh (Ω-cm$^2$) |
|---|---|---|---|---|---|---|---|---|---|
| pCz | pCz | 2.2 | 168 | 662.4 | 38.7 | 78.7 | 20.1 | 0.76 | 47242 |
| X2-9 | Epi-p1 | 2.3 | 150 | 632.4 | 37.3 | 76.7 | 18.1 | 0.82 | 2570 |
| X2-7 | Epi-p1 | 2.3 | 142 | 643.8 | 38.2 | 74.5 | 18.3 | 1.31 | 55209 |
| X2-5 | Epi-p1 | 2.4 | 144 | 649.3 | 38.2 | 75.9 | 18.8 | 0.98 | 37284 |
| X2-1 | Epi-p1 | 2.4 | 153 | 651.0 | 38.4 | 76.5 | 19.1 | 0.89 | 15033 |
| X2-15 | Epi-p2 | 3.4 | 183 | 662.8 | 38.8 | 76.8 | 19.7 | 1.00 | 4540 |
| X2-14 | Epi-p2 | 3.9 | 179 | 655.3 | 38.4 | 77.8 | 19.6 | 0.80 | 7240 |

The measured light IV data is shown in Table 13. A 20.1% efficiency was achieved on the p-type reference Cz PERC cell with $V_{oc}$ of 662 mV, $J_{sc}$ of 38.7 mA/cm$^2$ and $FF$ of 78.7%, which was among the best at the time (2013). The counter part epi-Si

cells showed efficiency of 18.1-19.1% with $V_{oc}$ of 632-651 mV on Epi-p1 material, and efficiency of 19.6-19.7% with $V_{oc}$ of 655-663 mV on Epi-p2 material.

Since all the wafers were processed at the same time, it is reasonable to assume that the front and back diffusion and passivation were similar for epi-Si and Cz wafers. Therefore, efficiency difference must come from the bulk properties. This was confirmed by the measured IQE data as shown in Figure 62. Measurement showed that the long wavelength IQE response of the Epi-p1 cell was much worse than the Cz and Epi-p2 cells. Exact reason for this is not fully understood but could be related to lower resistivity and bulk lifetime.

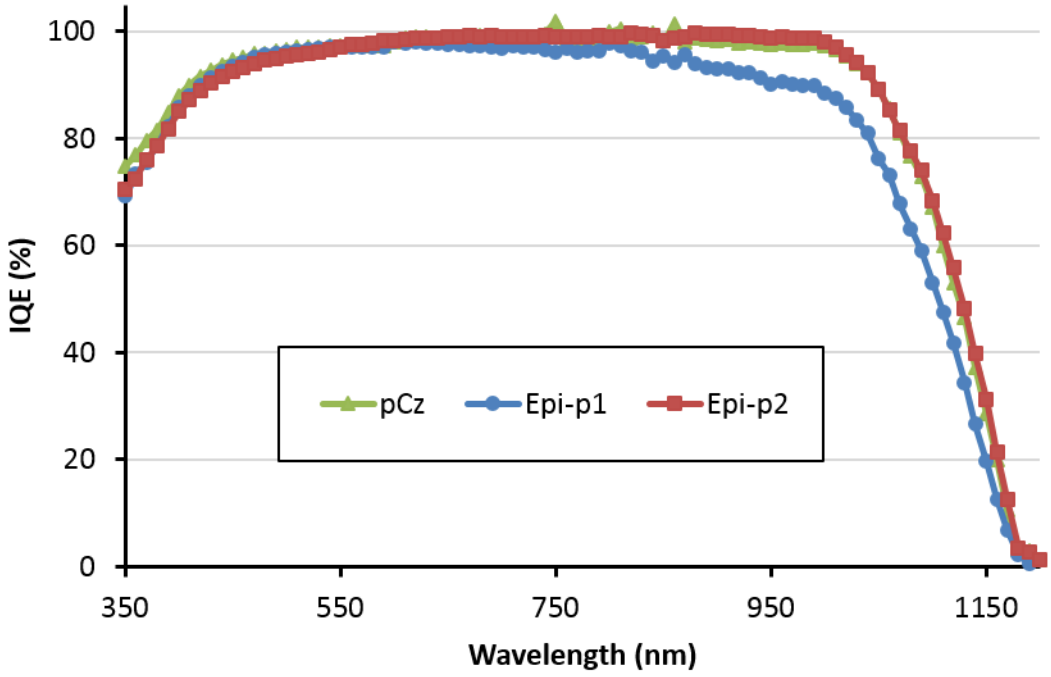



**Figure 62:** The measured IQE responses for the Cz, Epi-p1 and Epi-p2 materials.

Boron doped Cz cells are know to suffer light induced degradation (LID) in efficiency due to the formation of boron-oxygen complexes [104]. Since CVD deposited epi-Si wafers have much lower oxygen concentration than Cz, epi-Si cells are expected to show much lower LID in efficiency compared to the Cz cells. It has been shown that

epi-Si has oxygen concentration of $3\times10^{17}\text{cm}^{-3}$ compared to $\sim10^{18}\text{cm}^{-3}$ in Cz grown Si wafers [99]. To validate this claim, three epi-Si and Cz cells were measured before and after 48 hours of one-sun light exposure. Figure 63 Shows essentially 0% LID in the epi-Si cells compared to ~3.4% relative efficiency degradation in the Cz cells. In fact, Epi-p2 cells showed higher efficiency after LID even though their efficiency was ~0.3% lower than the Cz cells prior to LID.

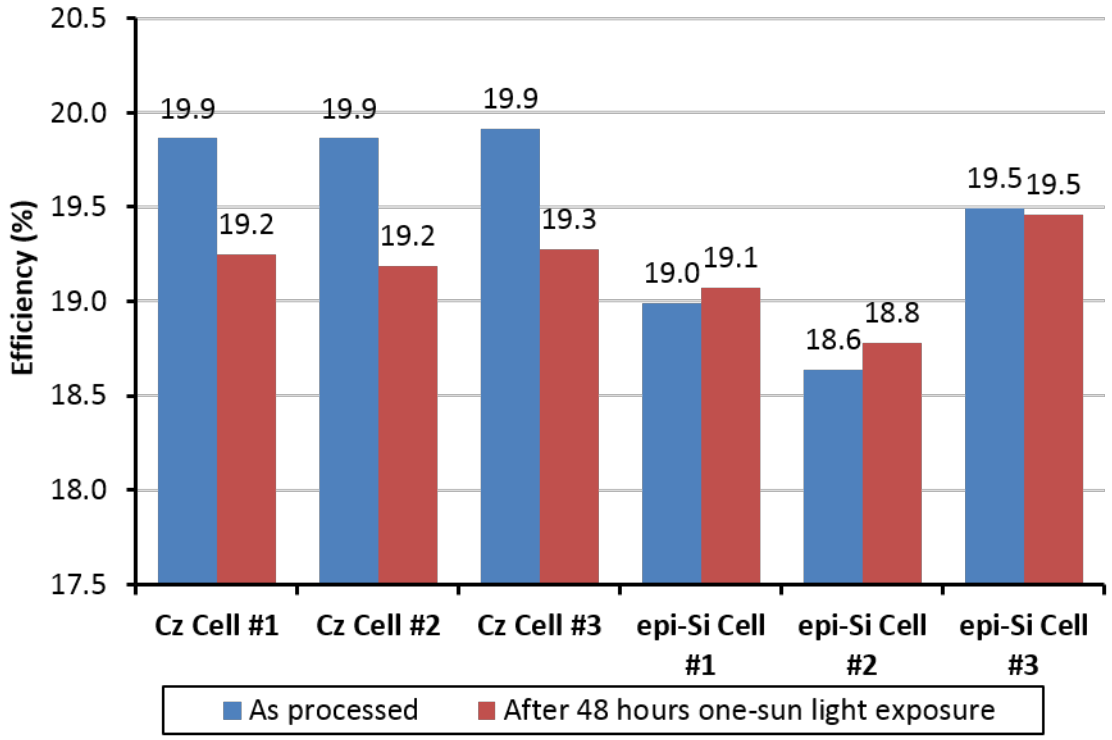



**Figure 63:** Cz and epi-Si wafer based PERC cells measured before and after 48 hours one-sun light exposure.

## *8.2 Extraction of Bulk Lifetime in the Finished p-type PERC Cells by Measurements and Modeling*

It is important to recognize that bulk lifetime can change during cell processing. It is more important to know what the lifetime is in the finished cells than the starting wafers in order to explain the difference in efficiency. In this section, we determined the bulk lifetime in finished cells by using the measured cell data and device modeling.

**Table 14:** The important PC1D and Sentaurus-2D modeling parameters for the screen-printed p-type PERC

| Parameter | PC1D pPERC | Sentaurus-2D pPERC |
|---|---|---|
| Front Reflectance | Measured | Ray-tracing |
| [1]Rf (%) | 92 | Ray-tracing |
| [2]Rb (%) | 96 | Ray-tracing |
| Thickness ($\mu$m) | 160 | 160 |
| Front Spacing (mm) | N/A | 2 |
| Front contact width ($\mu$m) | N/A | 126 |
| Back Spacing (mm) | N/A | 1 |
| Back contact width ($\mu$m) | N/A | 75 |
| Emitter Profile | Measured ($n^+$) | Measured ($n^+$) |
| Emitter sheet ($\Omega$/sq) | $\sim$90 ($n^+$) | $\sim$90 ($n^+$) |
| Base doping ($cm^{-3}$) | $6.5 \times 10^{15}$ (p) | $6.5 \times 10^{15}$ (p) |
| Base resistivity ($\Omega$-cm) | 2.2 (p) | 2.2 (p) |
| BSF Profile | N/A | $5 \times 10^{18}$-5$\mu$m ($p^+$) |
| BSF width ($\mu$m) | N/A | 85 |
| BSF sheet ($\Omega$/sq) | N/A | $\sim$26 ($p^+$) |
| FSRV (cm/s) | $10^4$ | $2 \times 10^3$ |
| FSRV-contact (cm/s) | N/A | $10^6$ |
| Lifetime ($\mu$s) | 500 | 500 |
| Diffusion Length ($\mu$m) | 1188 | 1188 |
| BSRV-Sn (cm/s) | 90 | 120 |
| BSRV-Sp (cm/s) | 7 | 7 |
| BSRV-contact (cm/s) | N/A | $10^6$ |
| Back Specific Contact Resistance (m$\Omega$-$cm^2$) | N/A | 2.6 |
| $R_s$ ($\Omega$-$cm^2$) | 0.75 | [3]0.25 |
| $R_{sh}$ ($\Omega$-$cm^2$) | 41666 | infinite |

[1]Rf: front internal reflectance. [2]Rb: back internal reflectance. [3]The $R_s$ here includes only busbar, finger and front contact resistance.

**Table 15:** The Measured and Modeled Light IV data for p-type PERC cell

| Device ID | $V_{oc}$ (mV) | $J_{sc}$ (mA /$cm^2$) | $FF$ (%) | Efficiency (%) |
|---|---|---|---|---|
| pCz | 662.4 | 38.7 | 78.7 | 20.1 |
| PC1D | 662.9 | 38.5 | 78.8 | 20.1 |
| Sentaurus-2D | 662.5 | 38.7 | 78.6 | 20.1 |

In order to extract the lifetime in the finished device, extensive 1D and 2D device modeling was done to match the measured device parameters as well as IQE. First, the 20.1% efficient reference p-type Cz PERC cells were used to obtain the match

between measured and modeled data. The important model parameters that gave this match are listed in Table 14. Lifetime was found to be 500 $\mu$s in a 2.2 $\Omega$-cm p-type finished Cz device. Although the 2D model characterizes the solar cell in more details, both models gave a very good match between modeled and measured light IV parameters (Table 14-15).

**Table 16:** Finished lifetime extracted by PC1D and Sentaurus for different epi-Si p-type materials

| Material | Resistivity and Thickness | Measured $V_{oc}$ (mV) | PC1D extracted Lifetime ($\mu$s) | Sentaurus extracted Lifetime ($\mu$s) |
|---|---|---|---|---|
| pCz | 2.2 $\Omega$-cm, 170 $\mu$m | 662 | 500 | 500 |
| epi-p1 | 2.4 $\Omega$-cm, 150 $\mu$m | 632-651 | 40-130 | 50-150 |
| epi-p2 | 3.7 $\Omega$-cm, 180 $\mu$m | 655-663 | 250-580 | 250-490 |

After matching the reference Cz cell, we changed only the material resistivity and thickness to extract the finished lifetime in the two epi-Si materials. Table 16 shows that Epi-p2 material had 250-580 $\mu$s bulk lifetime, while Epi-p1 has bulk lifetime of only 40-150 $\mu$s. This explains the slightly lower efficiency of epi-Si cells observed in this study compared to the Cz cells. In order to gain better insight into the two materials, we extended device modeling to generate the plot of cell efficiency as a function of bulk lifetime and resistivity using 170 $\mu$m wafer thickness, as shown in Figure 64. These curves indicate that for the PERC technology used in this research, both Cz and epi-Si material can benefit from higher bulk lifetime. In addition, the gap between the epi-Si and Cz cell can be explained primarily on the basis of bulk lifetime. Finally, the gap between the two materials can be bridged by improving the bulk lifetime or obtaining the right combination of lifetime and resisitivity.

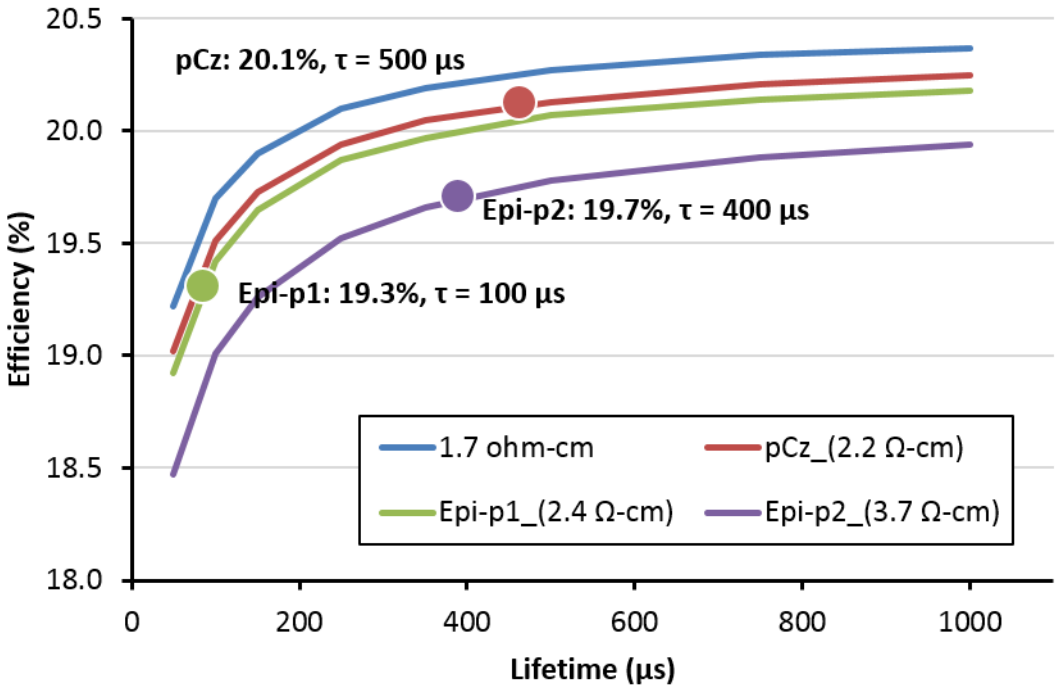



**Figure 64:** Sentaurus 2D modeling of p-type PERC cell efficiency as function of lifetime and resistivity for wafer thickness of 170 $\mu$m. Calculated cell efficiency for the three materials used in this study are shown by the dots.

## *8.3 Fabrication and Comparison of N-type PERT Cells on Epi-Si and Commercial Cz Si Wafers*

N-type Si solar cell has recently become a very active area of investigation because of its potential for higher cell efficiency [105]. Therefore, after comparing the p-type epi-Si and traditional Cz cells, we compared the n-type cells on the two materials. Like in the case of p-type cells, three different epi-Si wafers (Epi-n1: 2.9 Ω-cm/120 $\mu$m thick, Epi-n2: 12 Ω-cm/160 $\mu$m thick, and Epi-n3: 100 Ω-cm/180 $\mu$m thick) and a commercial grade Cz wafer (9.6 Ω-cm/160 $\mu$m thick) were used for the comparison. The screen-printed n-type PERT process [106, 107] developed in this research involved: (a) random pyramid texturing in a KOH based solution, (b) boron ion implantation with $3\times10^{15}$ B/cm$^2$ and energy of 10keV, (c) standard RCA clean, (d)

boron activation anneal at 1000°C with 60 minutes in nitrogen, (e) single side planarization in 9% KOH solution at 80°C for 13 minutes, (f) boron rich layer removal in a shaving solution (acid: nitric: HF = 100: 1: 1) for 210 sec., (g) phosphorous ion implantation with $2\times10^{15}$ P/cm$^2$ and energy of 10keV , (h) standard RCA clean, (i) anneal and thermal oxide passivation at 840°C with 60 minutes oxidation and 25 minutes nitrogen anneal, (j) PECVD $SiN_x$ front (620 sec.) and back (300 sec.), (k) screen printing of 27B Ag/Al paste on the front and H9412 Ag paste on the back in the form of dots array pattern with spacing of 500 $\mu$m and diameter of 100 $\mu$m, (l) contact firing in a belt furnace, (m) screen printing of low temperature PV 416 metal paste for back contact to connect the Ag dots. The n-type PERT cell structure is shown in Figure 65.

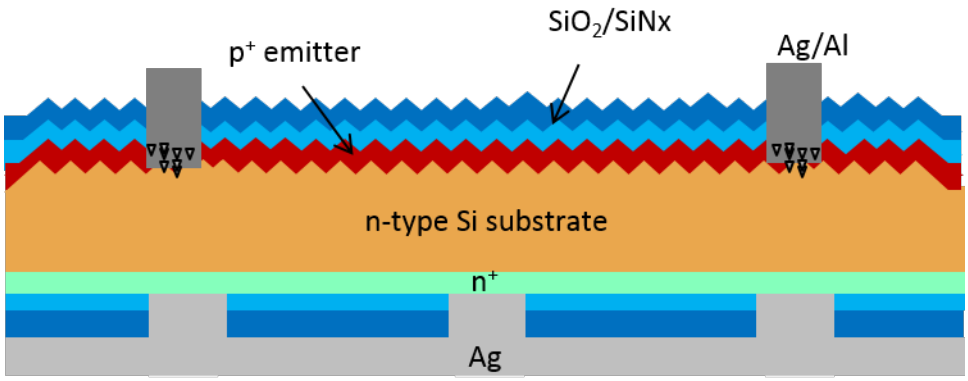



**Figure 65:** Schematic cross-section scheme of screen-printed n-type PERT cell.

The measured light IV data for the n-type PERT cells fabricated in this research is shown in Table 17. A 20.0% efficiency was achieved on the reference n-type Cz Si with $V_{oc}$ of 649 mV, $J_{sc}$ of 38.5 mA/cm$^2$ and $FF$ of 79.9%, which was among the best at the time (2013) [106, 107]. The counterpart epi-Si cells gave efficiency of 19.6-19.8% with $V_{oc}$ of 646-650 mV on Epi-n1 material, efficiency of 19.0-19.3% with $V_{oc}$ of 640-644 mV on Epi-n2 material, and efficiency of 18.9-19.5% with $V_{oc}$ of 639-644 mV on the Epi-n3 material.

Since all the wafers were processed at the same time, it is reasonable to assume that

**Table 17:** The measured LIV data for n-type PERT cell using Cz and epi-Si material

| Device ID | Material | Resis. (Ω-cm) | Thick. ($\mu$m) | $V_{oc}$ (mV) | $J_{sc}$ (mA /cm$^2$) | FF (%) | Eff. (%) | $R_s$ (Ω-cm$^2$) | Rsh (Ω-cm$^2$) |
|---|---|---|---|---|---|---|---|---|---|
| nCz | nCz | 9.6 | 160 | 648.8 | 38.5 | 79.9 | 20.0 | 0.65 | 8070 |
| XN1-14 | epi-n1 | 2.9 | 105 | 645.8 | 38.1 | 79.5 | 19.6 | 0.64 | 10500 |
| [1]XN1-4 | epi-n1 | 2.8 | 135 | 649.6 | 38.4 | 79.3 | 19.8 | 0.68 | 28441 |
| XN1-15 | epi-n2 | 6.8 | 169 | 639.5 | 38.3 | 77.7 | 19.0 | 0.66 | 9520 |
| XN1-16 | epi-n2 | 11.4 | 155 | 644.1 | 38.3 | 78.4 | 19.3 | 0.66 | 9530 |
| XN1-23 | epi-n2 | 18.9 | 163 | 641.8 | 38.3 | 78.2 | 19.2 | 0.69 | 6210 |
| XN1-24 | epi-n3 | 56 | 181 | 638.6 | 38.4 | 77.3 | 18.9 | 0.70 | 11400 |
| XN1-26 | epi-n3 | 113 | 179 | 643.7 | 38.6 | 78.3 | 19.5 | 0.68 | 11300 |
| XN1-27 | epi-n3 | 134 | 173 | 642.3 | 38.6 | 77.8 | 19.3 | 0.70 | 14600 |
| XN1-28 | epi-n3 | 132 | 170 | 642.5 | 38.2 | 77.6 | 19.1 | 0.71 | 11700 |

[1]This cell is using PVD [101] instead of screen-printed back contact process.

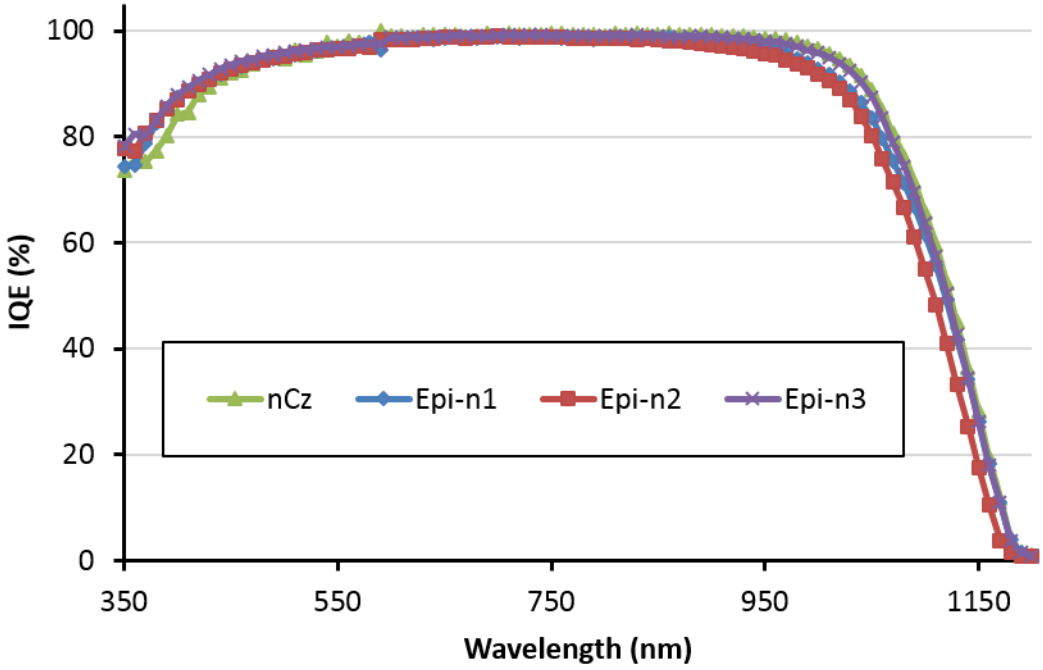



**Figure 66:** The measured IQE responses for the Cz, Epi-n1, Epi-n2 and Epi-n3 materials.

the front and back diffusion and passivation were similar for all the wafers. Therefore, the observed efficiency difference must have come from the bulk properties. However, there was virtually no difference in the long wavelength IQE response (Figure 66). This is probably because the $V_{oc}$ difference was too small (<5 mV) (Table 17) for all

the cells made in this study to show up in the long IQE response.

## *8.4 Extraction of Bulk Lifetime in the Finished Cells by Measurements and Modeling*

**Table 18:** The important PC1D and Sentaurus-2D modeling parameters for the screen-printed n-type PERT cell

| Parameter | PC1D nPERT | Sentaurus-2D nPERT |
|---|---|---|
| Front Reflectance | Measured | Ray-tracing |
| [1]Rf (%) | 92 | Ray-tracing |
| [2]Rb (%) | 93 | Ray-tracing |
| Thickness ($\mu$m) | 160 | 160 |
| Front Spacing (mm) | N/A | 1.5 |
| Front contact width ($\mu$m) | N/A | 112.5 |
| Back Spacing (mm) | N/A | 0.5 |
| Back contact width ($\mu$m) | N/A | [4]24.2 |
| Emitter Profile | Measured ($p^+$) | Measured ($p^+$) |
| Emitter sheet ($\Omega$/sq) | ~90 ($p^+$) | ~90 ($p^+$) |
| Base doping ($cm^{-3}$) | $4.7 \times 10^{14}$ (n) | $4.7 \times 10^{14}$ (n) |
| Base resistivity ($\Omega$-cm) | 9.6 (n) | 9.6 (n) |
| BSF Profile | Measured ($n^+$) | Measured ($n^+$) |
| BSF width ($\mu$m) | N/A | Cell width |
| BSF sheet ($\Omega$/sq) | ~74 ($n^+$) | ~74 ($n^+$) |
| FSRV (cm/s) | $10^4$ | $5.4 \times 10^3$ |
| FSRV-contact (cm/s) | N/A | $10^6$ |
| Lifetime ($\mu$s) | 1200 | 1200 |
| Diffusion Length ($\mu$m) | 1201 | 1201 |
| BSRV-Sn (cm/s) | $5 \times 10^4$ | $5 \times 10^4$ |
| BSRV-Sp (cm/s) | $5 \times 10^4$ | $5 \times 10^4$ |
| BSRV-contact (cm/s) | N/A | $10^6$ |
| Back Specific Contact Resistance (m$\Omega$-cm$^2$) | N/A | 6 |
| $R_s$ ($\Omega$-cm$^2$) | 0.5 | [3]0.27 |
| $R_{sh}$ ($\Omega$-cm$^2$) | 8070 | infinite |

[1]Rf: front internal reflectance. [2]Rb: back internal reflectance. [3]The $R_s$ here includes only busbar, finger and front contact resistance. [4]24.2 $\mu$m width 500$\mu$m spacing line contact has almost the same metal coverage as experimental 110 $\mu$m diameter 500 $\mu$m spacing point contact.

It is important to recognize that bulk lifetime can change appreciably in n-type Si during cell processing due to boron diffusion and its activation at much higher temperature (1000-1050°C). In order to extract the bulk lifetime in finished cells, we

**Table 19:** The measured LIV data for p-type PERC cell using Cz and epi-Si material

| Device ID | $V_{oc}$ (mV) | $J_{sc}$ (mA /cm$^2$) | $FF$ (%) | Efficiency (%) |
|---|---|---|---|---|
| nCz | 648.8 | 38.5 | 79.9 | 20.0 |
| PC1D | 649.1 | 38.5 | 80.0 | 20.0 |
| Sentaurus-2D | 648.8 | 38.5 | 80.0 | 20.0 |

used the same measurement and modeling methodology as in section 8.2. First, we matched the 20% n-type PERT Cz cell using PC1D as well as Sentaurus-2D device models. The important model parameters are listed in Table 18. A bulk lfetime of 1.2 ms in a 9.6 Ω-cm n-type Cz material was obtained in the finished device.

After matching the reference Cz n-type PERT cell (Table 18-19), we inserted the correct resistivity and thickness for epi-Si cells and varied only the bulk lifetime to match $V_{oc}$ and cell performance. The extracted bulk lifetimes which gave excellent match between the measured and modeled cell data are shown in Table 20. The bulk lifetime in these epi-Si cells was found to be lower than the Cz material, which explains the slightly lower efficiency of epi-Si cells compared to the Cz cells in this study.

**Table 20:** Finished lifetime extracted by PC1D and Sentaurus for different epi-Si n-type materials

| Material | Resistivity and Thickness | Measured $V_{oc}$ (mV) | PC1D extracted Lifetime ($\mu$s) | Sentaurus extracted Lifetime ($\mu$s) |
|---|---|---|---|---|
| nCz | 9.6 Ω-cm, 160$\mu$m | 649 | 1200 | 1200 |
| epi-n1 | 2.9 Ω-cm, 120$\mu$m | 646-650 | 280-780 | 300-940 |
| epi-n2 | 12 Ω-cm, 160$\mu$m | 640-644 | 200-330 | 210-370 |
| epi-n3 | 100 Ω-cm, 180$\mu$m | 639-644 | 200-330 | 200-340 |

Next, we extended device modeling to generate a plot of cell efficiency as function of bulk lifetime and resistivity using wafer thickness of 160 $\mu$m, as shown in Figure 67. These curves indicate that for the PERT technology used in this research, both Cz

and epi-Si material can benefit from higher bulk lifetime. In addition, the gap between the epi-Si and Cz cell can be explained primarily on the basis of bulk lifetime. Finally, the gap between the two materials can be bridged by improving the bulk lifetime or obtaining the right combination of lifetime and resistivity. This conclusion is quite similar to what was found in the p-type cells.

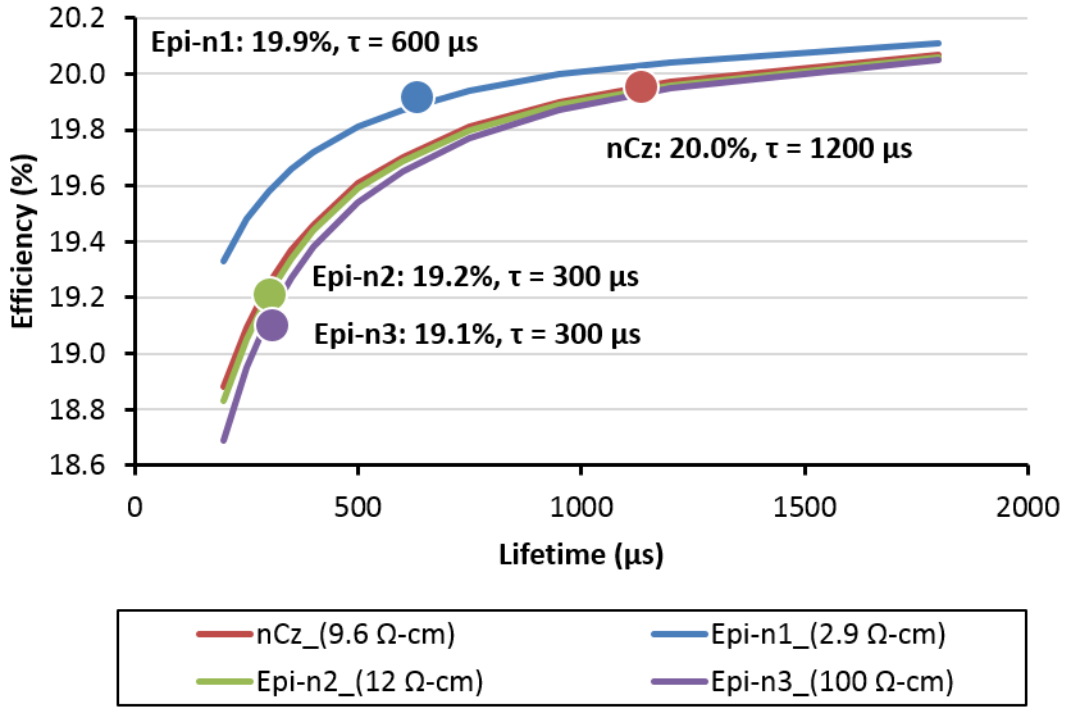



**Figure 67:** Sentaurus 2D modeling of n-type PERT cell efficiency as function of lifetime and resistivity for wafer thickness of 160 $\mu$m. Calculated cell efficiency for the four materials used in this study are shown by the dots.

## *8.5 Summary*

In this task, high efficiency (~20%) screen-printed Si solar cells were fabricated on both p-type and n-type epi-Si Kerfless wafers with thickness of 120-180 $\mu$m. Different resistivity (2-10 Ω-cm) p-type and n-type epi-Si wafers were tested. Best p-type PERC cell efficiency of 19.7% was achieved on ~180 $\mu$m epi-Si wafers with resistivity of ~3.7 Ω-cm while the counter part commercial Cz cell gave 20.1% efficiency. In the case of

n-type PERT cell, best efficiency of 19.8% was achieved on ∼120 $\mu$m epi-Si wafers with resistivity of ∼2.9 Ω-cm while the counter part Cz cell gave 20.0% efficiency on 160 $\mu$m thick Si. Finished bulk lifetime was analyzed by IQE measurement and device modeling. Some epi-Si materials gave bulk lifetime close to Cz; however, in most cases bulk lifetime was somewhat lower than the Cz material. The gap between the epi-Si and Cz cells can be explained primarily on the basis of resistivity and bulk lifetime. Finally, model calculations showed that the cell efficiency can be improved appreciably by improving the bulk lifetime or obtaining the right combination of lifetime and resisitivity for the diffusion and screen-printed technology used in this study.

# CHAPTER IX

# TASK 5: DEVELOPMENT OF ADVANCED HIGH EFFICIENCY LARGE AREA SCREEN-PRINTED SOLAR CELLS ON DIRECT KERFLESS EPITAXIALLY GROWN MONO-CRYSTALLINE SI WAFER

This chapter demonstrates the potential of epitaxially grown Si (epi-Si) wafers with doped layers for high efficiency solar cells. Boron doped 239 $cm^2$ 180-200 $\mu$m thick 2 $\Omega$-cm wafers were grown with and without 15 $\mu$m thick $p^+$ layer with a doping of $5\times10^{17}$ $cm^{-3}$. A layer transfer process involving porous Si layer to lift off epi-Si wafers from the reusable substrate was used. The $pp^+$ wafers were converted into $n^+pp^+$ PERT (passivated emitter, rear totally-diffused) cells by forming an oxide passivated $n^+$ emitter on front and oxide/nitride passivated epitaxially grown (epi-grown) $p^+$ BSF on the entire back with local screen-printed contacts to BSF. To demonstrate and quantify the benefit of the epi-grown $p^+$ layer, standard PERC (passivated emitter and rear cell) cells with local BSF and contacts were also fabricated on p-type epi-grown Si wafers as well on commercial grade Cz wafers without the $p^+$ region. In addition, Sentaurus 2D device model was used to assess the impact of the epi-grown $p^+$ layer, which showed an efficiency gain of $\sim$0.5% for this PERT structure over the traditional PERC cell. This was validated by the cell results which showed higher performance for PERT structure with an efficiency of $\sim$20.1% for the PERC and $\sim$20.3% for the PERT cells using epi-Si wafers. Both modeling and experimental data showed that the reason for this efficiency difference was higher $FF$ in PERT cells due to the decrease in lateral resistance on the rear side. It is important to note

that efficiency gain due to higher $FF$ was greater than the recombination loss in the $p^+$ layer because of the selected BSF design with lighter doping and thicker epi-grown $p^+$ region. Finally, a three-layer-epi PERT (eptiaxially grown emitter, base and BSF) cell design with both front and back built-in junctions is proposed for much higher cell efficiency. Both p-type front junction and n-type back junction 3-layer-epi PERT cells were modeled. It is shown that screen printing of 40 $\mu$m wide lines ($\sim$2.3% metal coverage) in combination with thinner floating busbars ($\sim$3.8% total shadow loss) and improved bulk material (1.7 $\Omega$-cm, 1 ms lifetime for p-type base and 10 $\Omega$-cm, 3 ms lifetime for n-type base) can give 3-layer-epi PERT cell efficiency of >22.7%.

Although cells made from the thick epi-Si wafers gave lower efficiency compared to Cz wafers in Chapter VIII (Task 4) due to somewhat lower bulk lifetime. Since then, our collaborator, Crystal Solar Inc., has improved their reactor and deposition conditions to reduce defects and impurities to achieve higher lifetime for both n-type and p-type epi-Si wafers. All the epi-Si cells reported in this chapter were made from these next generation epi-Si wafers with comparable or higher bulk lifetime relative to the counterpart Cz wafers.

## *9.1 Fabrication and 2D Sentaurus Modeling of >20% Efficient P-type PERC Cell*

Sentaurus 2D Device model [29] was used to understand the loss mechanisms and estimate the efficiency potential of epi-grown $pp^+$ structure with optimized $p^+$ layer. The physical models recommended by Pietro P. Altermatt [28] were selected for the Sentaurus device modeling, including Fermi-Dirac Statistics, Klaassens unified mobility model, Schenk bandgap narrowing model and Auger recombination coefficient from Dziewior and Schmid. We first fabricated and modeled a 20.1% screen-printed p-type PERC cell on Cz using the relevant experimental inputs as shown in Table 21. The process details are described in Section 9.3. Figure 68 shows the schematic of the cross-section of the unit cell used for 2D modeling of this PERC structure. The front

contacts (spacing of 1.75 mm) are symmetrically positioned with respect to the back contacts (spacing of 1 mm). We applied and used floating busbars to fabricate and model these cells. Since we used floating busbars which do not make direct contact to Si, we reduced the metal/Si contact area to 3.4% (corresponding to 60 $\mu$m wide fingers without busbar) in the model but kept the shading to 6.3% (grid finger lines + busbars).

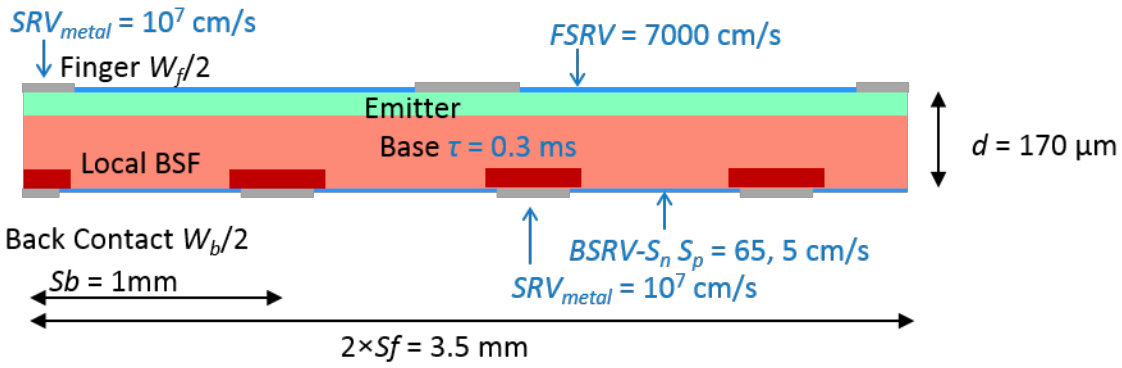



**Figure 68:** Schematic of the cross-section of the unit cell of p-type PERC cell used for Sentaurus 2D modeling.

Using the Sentuarus model and emitter doping profile (Figure 69 a), first, a plot of $J_{oe}$ vs $FSRV$ (Figure 69 b) was generated [22, 23, 21]. Then the Front Surface Recombination Velocity ($FSRV$) of 7000 cm/s was extracted from the measured $J_{oe}$ of 74 fA/cm$^2$ on a symmetric test structure prepared with the same emitter and passivation scheme on both sides.

Bulk lifetime of 300 $\mu$s was used for commercial grade p-type Cz wafer in this study [108]. For modeling local Al BSF, the BSF profile was approximated to be 1.2 $\mu$m deep with uniform-doping of $5\times10^{18}$ cm$^{-3}$ which is close to the expected profile and also corresponds to the measured $J'_{ob.cont}$ ~900 fA/cm$^2$ [109]. $R'_s$ in Table 21 represents the series resistance contribution from front contact, finger and busbar, which excludes the base and emitter sheet resistance components calculated by the model.

**Table 21:** The important Sentaurus-2D modeling parameters for the screen-printed p-type PERC cell

| Sentaurus Parameters | 20.1% Cz-p PERC Cell |
|---|---|
| Thickness $d$ ($\mu$m) | 170 |
| Front Contact Spacing $S_f$ (mm) | 1.75 |
| Front Contact Width $W_f$ ($\mu$m) | 60 (3.4%) |
| Front Shading Width ($\mu$m) | 110 (6.3%) |
| Emitter Profile | Measured, 0.45 $\mu$m |
| Emitter Surface Concentration (cm$^{-3}$) | $9\times10^{19}$ |
| Emitter Sheet Resistance ($\Omega$/sq) | $\sim$75 |
| Base Doping (cm$^{-3}$) | $8.6\times10^{15}$ |
| Base Resistivity ($\Omega$-cm) | 1.7 |
| Back Contact Spacing $S_b$ (mm) | 1 |
| Back Contact Width $W_b$ ($\mu$m) | 75 |
| Al Local BSF Profile | $5\times10^{18}$, 1.2 $\mu$m |
| Al Local BSF Width ($\mu$m) | 77.4 |
| Front Surface Recombination Velocity $FSRV$ (cm/s) | 7000 |
| Contact Surface Recombination Velocity $SRV_{metal}$ (cm/s) | $10^7$ |
| Lifetime $\tau$ ($\mu$s) | 300 |
| Back Surface Recombination Velocity $BSRV$-$S_n$ $S_p$ (cm/s) | 65, 5 |
| Back Contact Specific Contact Resistance (m$\Omega$-cm$^2$) | 2.6 |
| Series Resistance for Front Contact, Fingers and Busbars $R'_s$ ($\Omega$-cm$^2$) | 0.42 |

It has been shown that in an oxide passivated PERC cell, back surface recombination velocity ($BSRV$) can become a function of injection level as the injection level transitions from low to high. This increases ideality factor and lowers $FF$ [110]. This phenomenon attributed to the combination of oxide charge and asymmetric $S_p/S_n$ ratio of <1 in the literature [111, 112, 113]. Therefore, to model the rear dielectric passivation of our oxide passivated PERC cell more accurately, we first determined the effective Back Surface Recombination Velocity ($S_{eff}$) on a symmetric test structure with oxide/nitride surface passivation on both sides. This was done by first measuring effective lifetime ($\tau_{eff}$) on the symmetric structure as a function of injection level using the Sinton tester [114] and then calculating $S_{eff}$ as a function of injection level

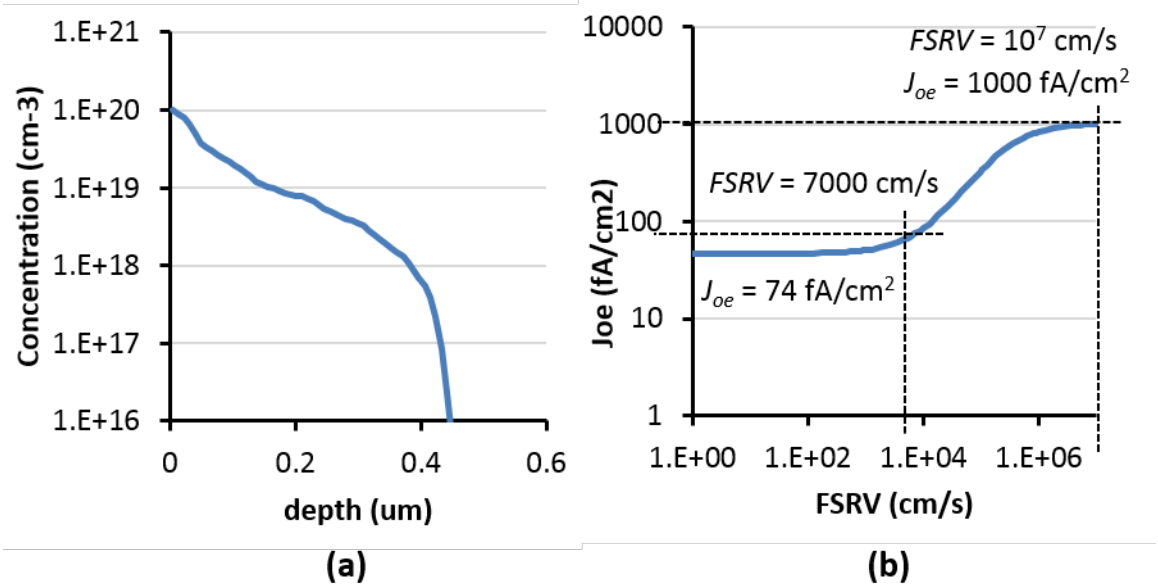



**Figure 69:** (a) Measured phosphorus doping profile. (b) Modeled $J_{oe}$ vs $FSRV$ curve from Sentaurus model.

from equation (55) using bulk lifetime ($\tau_{bulk}$) of 300 $\mu$s and wafer thickness ($d$) of 150 $\mu$m.

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + 2 \times \frac{S_{eff}}{d} \tag{55}$$

The calculated $S_{eff}$ as function of injection level for our dielectric stack is shown in Figure 70. Next, we used a single trap SRH model (equation 56) for surface recombination to match the measured $S_{eff}$ data by varying $S_n$ and $S_p$ values, instead of using detailed dielectric parameters [115, 111].

$$S_{eff} \equiv \frac{U_s}{\Delta n}, \text{ with } \quad U_s = \frac{S_p S_n (pn - n_i^2)}{S_p(p + n_i e^{-E_t/kT}) + S_n(n + n_i e^{-E_t/kT})} \tag{56}$$

We were able to obtain a good match between the calculated and measured injection level dependence in the range of $10^{14}$ and $2{\times}10^{15}$ cm$^{-3}$ using $S_n = 65$ cm/s, $S_p = 5$ cm/s, for a mid-gap trap $E_t = 0$ as shown in Figure 70. With these $S_n$ and $S_p$ values in the model, a good match was obtained between the modeled and experimental data for the 20.1% efficient PERC cell (Table 21 and 22).

In order to see the impact of $S_n$ and $S_p$ on cell efficiency and n-factor, we varied

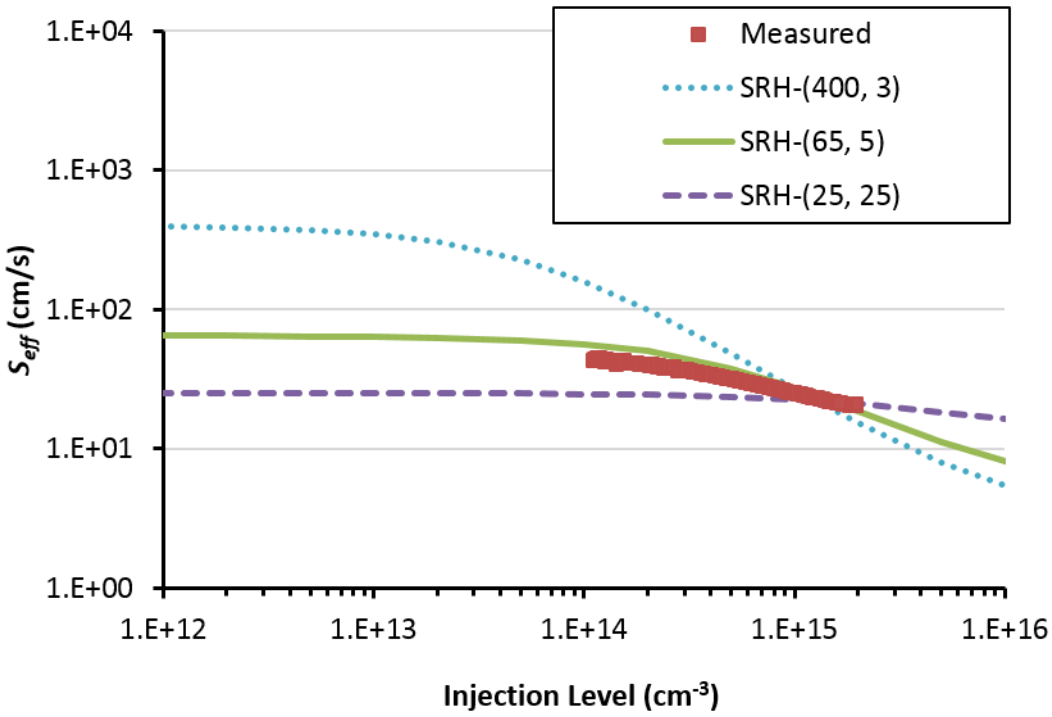



**Figure 70:** Measured $S_{eff}$ as function of injection level for the surface passivation by thin thermal oxide/ PECVD $SiN_x$ stack on top of p-type wafer. The calculated $S_{eff}$ as function of injection level using equation (2) with ($S_n$, $S_p$) = (400, 3), (65, 5), and (25, 25) cm/s are also plotted for comparison.

the combination of the two in Table 22. Table 22 and Figure 70 together show the impact of $S_n$ and $S_p$ and their ratio on the injection level dependence of effective bulk lifetime and cell efficiency. When $S_n = S_p$, there is no/little injection level dependence, n-factor is low (1.03) with high $FF$ of 79.8 and efficiency of 20.3%. However, $S_n \gg S_p$ results in different effective lifetime at $V_{mp}$ (injection level $\sim 10^{14}$ cm$^{-3}$) compared to $V_{oc}$ (injection level $\sim 10^{15}$ cm$^{-3}$) and degrades the ideality factor, $FF$ and cell efficiency. Figure 70 shows that combination of $S_n$ = 400 cm/s and $S_p$ = 3 cm/s gave higher $S_{eff}$ (lower effective lifetime) $V_{mp}$ compared to $V_{oc}$, which increased the n-factor from 1.08 to 1.23, reduced the $FF$ from 79.3% to 77.8% and lowered the efficiency from 20.2% to 19.5% (Table 22).

**Table 22:** The Measured and Modeled LIV data for p-type PERC cell using different $S_n$ and $S_p$

| ID | $S_n$, $S_p$ (cm/s) | $V_{oc}$ (mV) | $J_{sc}$ (mA /cm$^2$) | $FF$ (%) | Eff. (%) | n-factor | $R_s$ ($\Omega$-cm$^2$) |
|---|---|---|---|---|---|---|---|
| Experiment | n/a | 662 | 38.5 | 78.7 | 20.1 | 1.07 | 0.67 |
| Model | 65, 5 | 660 | 38.5 | 79.3 | 20.2 | 1.08 | 0.76 |
| Model | 400, 3 | 660 | 38.1 | 77.8 | 19.5 | 1.23 | 0.76 |
| Model | 25, 25 | 660 | 38.6 | 79.8 | 20.3 | 1.03 | 0.76 |

## *9.2 2D Sentaurus Modeling of P-type PERT Cells*

After establishing the Sentaurus model for our PERC cells, including the injection level dependence of $S_{eff}$, we modeled the PERT cell with different BSF profiles while keeping all other parameters constant. The schematic of p-PERT cross-section is shown in Figure 71. Unlike the PERC cell, the back surface of the PERT cell is always in low level injection ($LLI$) during the cell operation under 1 sun because of $p^+$ doping $>10^{17}$ cm$^{-3}$. ($<10^{15}$ cm$^{-3}$ injection level compared to BSF surface doping of $>10^{17}$cm$^{-3}$). According to equation (56), under $LLI$, $S_{eff} \approx S_n$. We used the $S_n$ versus $N_s$ data (Figure 72) of Hoex et al. [10, 16] for thermal oxide passivated boron doped surfaces for our modeling.

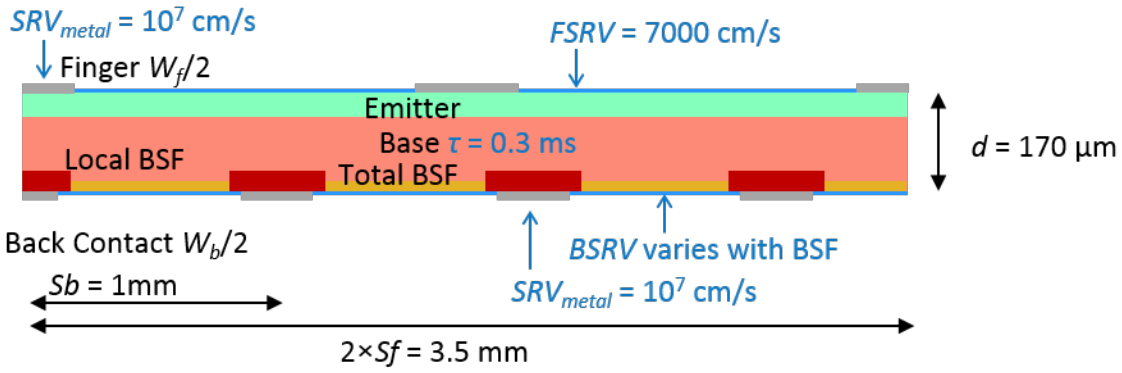



**Figure 71:** Schematic of the cross-section of the unit cell of p-type PERT used for Sentaurus 2D modeling.

PERT cell efficiency was modeled for various $p^+$ BSF designs as shown in Figure

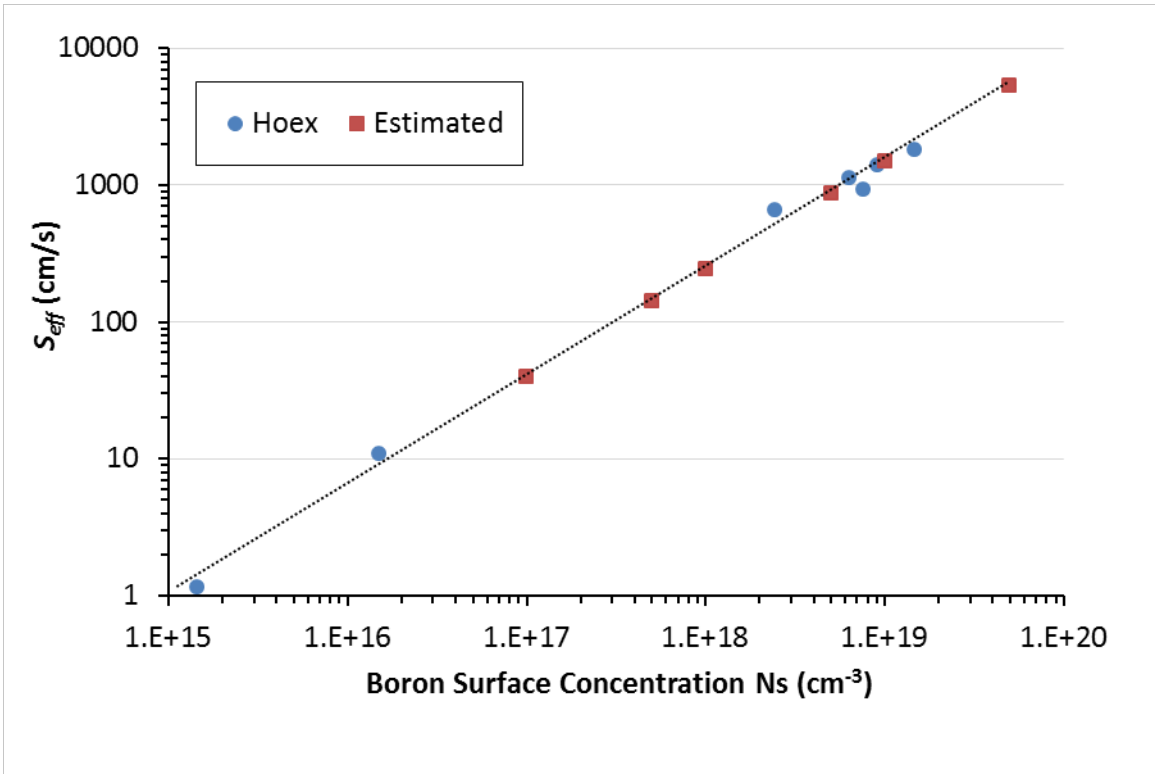
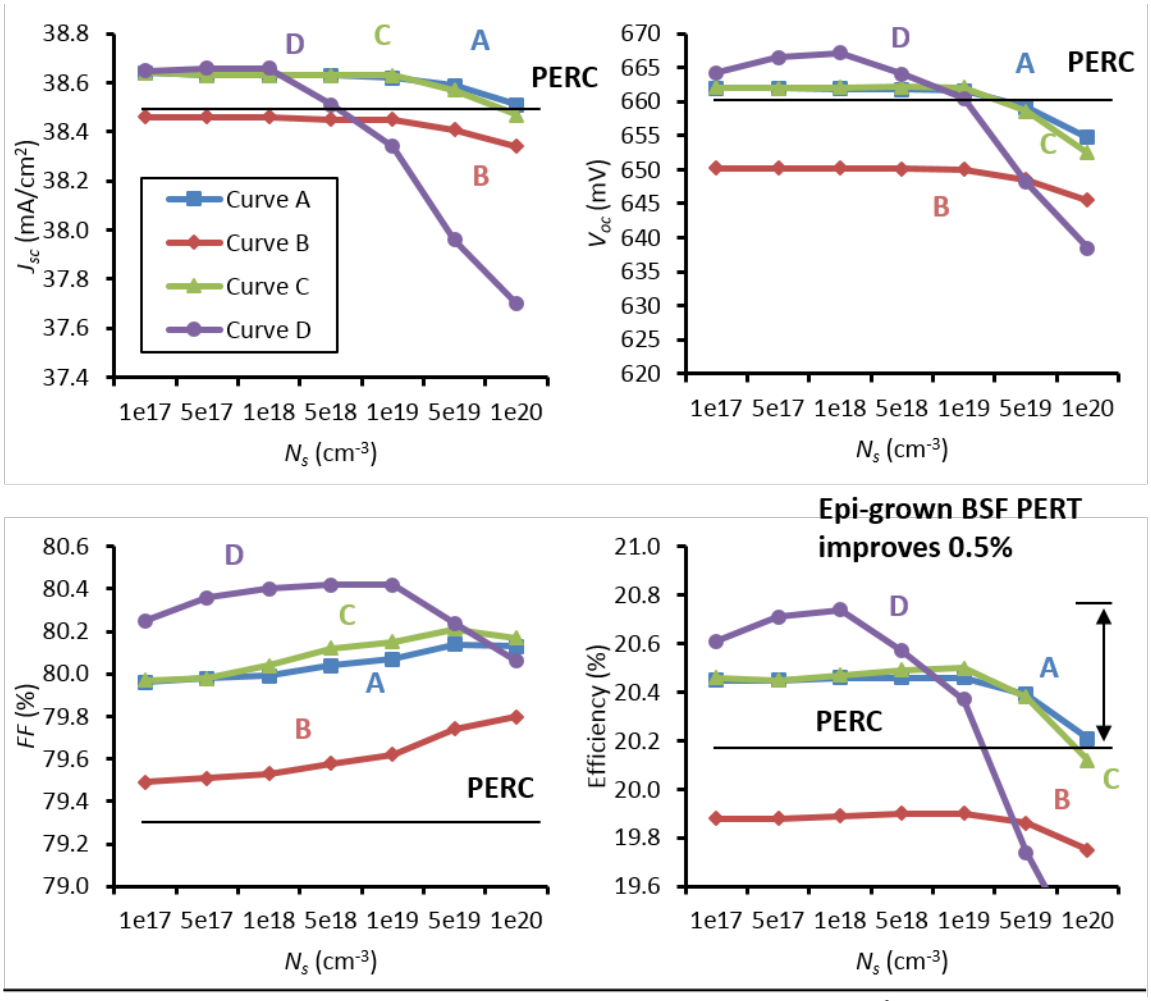



**Figure 72:** The reported and estimated $S_{eff}$ data as function of Boron doped surface passivated by $SiO_2$ [24].

73. Note that for each $p^+$ profile, $N_s$ was varied from $10^{17}$ to $10^{20}$ $cm^{-3}$ to optimize the BSF design. The modeled 20.2% PERC data (Table 22) is also plotted as a reference in Figure 73 to facilitate the comparison between PERC and PERT cells.

Curve A shows that a 0.5 $\mu$m deep Gaussian BSF profile in PERT cell can give higher efficiency than the modeled 20.2% PERC cell for all surface doping concentrations provided 300 $\mu$s lifetime can be maintained during the high temperature boron diffusion. However, if the lifetime drops to 100 $\mu$s during high temperature diffusion ($\geq$ 1000 °C), as suggested by some investigators [116, 117] for p-type Cz material, then the PERT cell will become inferior to the PERC cell (Curve B). Curve C in Figure 73 shows that if 1.1 $\mu$m deep Gaussian BSF profile is used, then PERT cell efficiency will become inferior to PERC cells for $N_s$ greater than $10^{20}$ $cm^{-3}$. This is because Auger recombination in the BSF region becomes too high. Thus maintaining bulk lifetime




| Curve | BSF Profile | $N_s$ (cm$^{-3}$) | Junction Depth (µm) | Lifetime (µs) |
|---|---|---|---|---|
| A | Gaussian | Varied | 0.5 | 300 |
| B | Gaussian | Varied | 0.5 | 100 |
| C | Gaussian | Varied | 1.1 | 300 |
| D | Uniform | Varied | 15 | 300 |

**Figure 73:** Modeled LIV data with different BSF profiles in PERT solar cells.

and selecting the BSF profile are critical for higher PERT cell efficiency compared to the PERC cell. Finally, Curve D in Figure 73 shows that for an epi-grown 15 $\mu$m thick BSF, optimum doping is $< 10^{18}$ cm$^{-3}$ resulting in ~0.5% higher efficiency than the counterpart PERC cell. In Figure 73, efficiency first increases with doping because of the decrease in sheet resistance which results in higher $FF$. Efficiency decreases at higher doping because increased doping increases Auger recombination

and lowers $J_{sc}$ and $V_{oc}$ which offsets the gain in $FF$.

Next, we calculated the impact of thickness of epi-grown uniform BSF. Figure 74 shows a broad maxima with best efficiency achieved in the thickness range of 15-30 $\mu$m with doping $<10^{18}$ cm$^{-3}$. Note that the PERT cell efficiency starts to decrease rapidly with increased BSF thickness for doping $>10^{18}$ cm$^{-3}$ because Auger recombination becomes dominant. Table 23 shows that the modeled 0.5% efficiency improvement of the PERT cell results from 0.18% increase in efficiency from $V_{oc}$, 0.09% increase in efficiency from $J_{sc}$, and 0.23% increase in efficiency from $FF$.

Table 23 also summarizes the change in various components of $J_{ob}$ that account

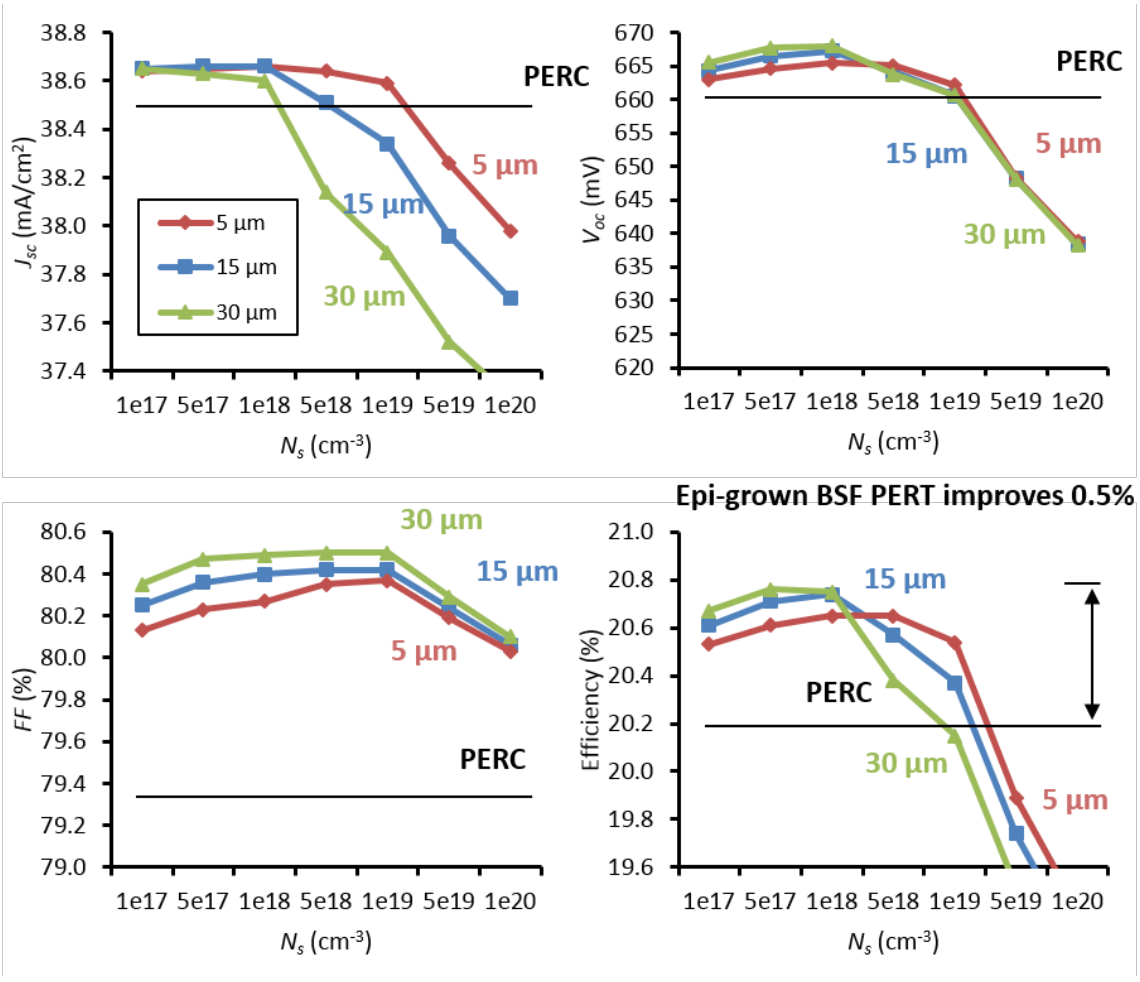



**Figure 74:** Modeled LIV data with different thickness uniform BSF profiles in PERT solar cells. Lifetime was kept as 300 $\mu$s in the modeling.

**Table 23:** Detailed comparison between modeled PERC and PERT solar cell with deep lightly doped BSF

| Parameter | 20.2%-PERC | 20.7%-PERT |
|---|---|---|
| $V_{oc}$ (mV) | 660 | 667 |
| $J_{sc}$ (mA/cm$^2$) | 38.5 | 38.7 |
| $FF$ | 79.3 | 80.4 |
| Efficiency (%) | 20.2 | 20.7 |
| n-factor | 1.08 | 1.02 |
| Total $R_s$ ($\Omega$-cm$^2$) | 0.76 | 0.70 |
| [1]Total $J_o$ (fA/cm$^2$) | 275 | 212 |
| [1]Total $J_{oe}$, $J_{oe.metal}$, $J_{oe.field}$ (fA/cm$^2$) | 106, 72, 34 | 106, 72, 34 |
| [1]$J_{ob.bulk}$ (fA/cm$^2$) | 74 | 67 |
| [1]Total $J'_{ob}$, $J'_{ob.metal}$, $J'_{ob.field}$ (fA/cm$^2$) | 95, 68, 27 | 39, 25, 14 |

[1]Total $J_o$ = total $J_{oe}$ + total $J_{ob}$. Total $J_{oe} = J_{oe.metal} + J_{oe.field}$. Total $J_{ob} = J_{ob.bulk}$ + total $J'_{ob} = J_{ob.bulk}$ + $J'_{ob.metal}$ + $J'_{ob.field}$.

for the 7 mV increase in $V_{oc}$ in the PERT cell. Because of the 15 $\mu$m thick p$^+$ region, the base of the PERT device was 155 $\mu$m thick as opposed to 170 $\mu$m. This reduced $J_{ob.bulk}$ from 74 to 67 fA/cm$^2$. Metal contribution to $J_{ob}$ also reduced significantly from 68 to 25 fA/cm$^2$ due to the presence of heavily doped p$^+$ region underneath the metal. Finally, $J_{ob}$ of the field region between the metal contacts reduced from 27 to 14 fA/cm$^2$ because of superior oxide/p$^+$ passivation, which does not exhibit injection level dependence. This was supported by the decrease in extracted $S_{eff}$ value from 25 in the PERC to 13 cm/s for the PERT cell. Increase in $FF$ is due to the combination of reduced lateral resistance on the back, which lowers total $R_s$ from 0.76 to 0.70 $\Omega$-cm$^2$, and a decrease in n-factor from 1.08 to 1.02 because of elimination of injection level dependence of $S_{eff}$. It is important to recognize that such deep and lightly doped layer (>15 $\mu$m, <$10^{18}$ cm$^{-3}$) can be only achieved by the epitaxial technology because most traditional diffusion technologies give $N_s \geq 10^{19}$ cm$^{-3}$ and junction depth of $<\sim 3\mu$m for reasonable drive-in time. Using these guidelines, $\sim$2 $\Omega$-cm epi-Si wafers were grown with and without the 15 $\mu$m thick p$^+$ layer and converted into PERC and PERT cells to validate the model.

## *9.3 Fabrication of p-type PERC and PERT Solar Cell*

Large area (239cm$^2$) p and pp$^+$ substrates were grown by epitaxy using the layer transfer technology developed at Crystal Solar Inc. [6]. PERT and PERC cells were fabricated on these 180-200 $\mu$m thick substrates. A commercial Cz wafer was used for reference on which PERC cells were made. All the cells were fabricated simultaneously with no change in the process sequence shown in Figure 75. The base resistivity of both Cz and epi-Si wafers was $\sim$2 $\Omega$-cm. The in-situ p$^+$ boron doped BSF layer was 15 $\mu$m thick with uniform doping in range of $10^{17} \sim 10^{18}$ cm$^{-3}$. Cell sturcutre included $POCl_3$ diffused emitter, thin thermal-$SiO_2/SiN_x$ passivation on both surfaces, and local Al BSF contact on the back.

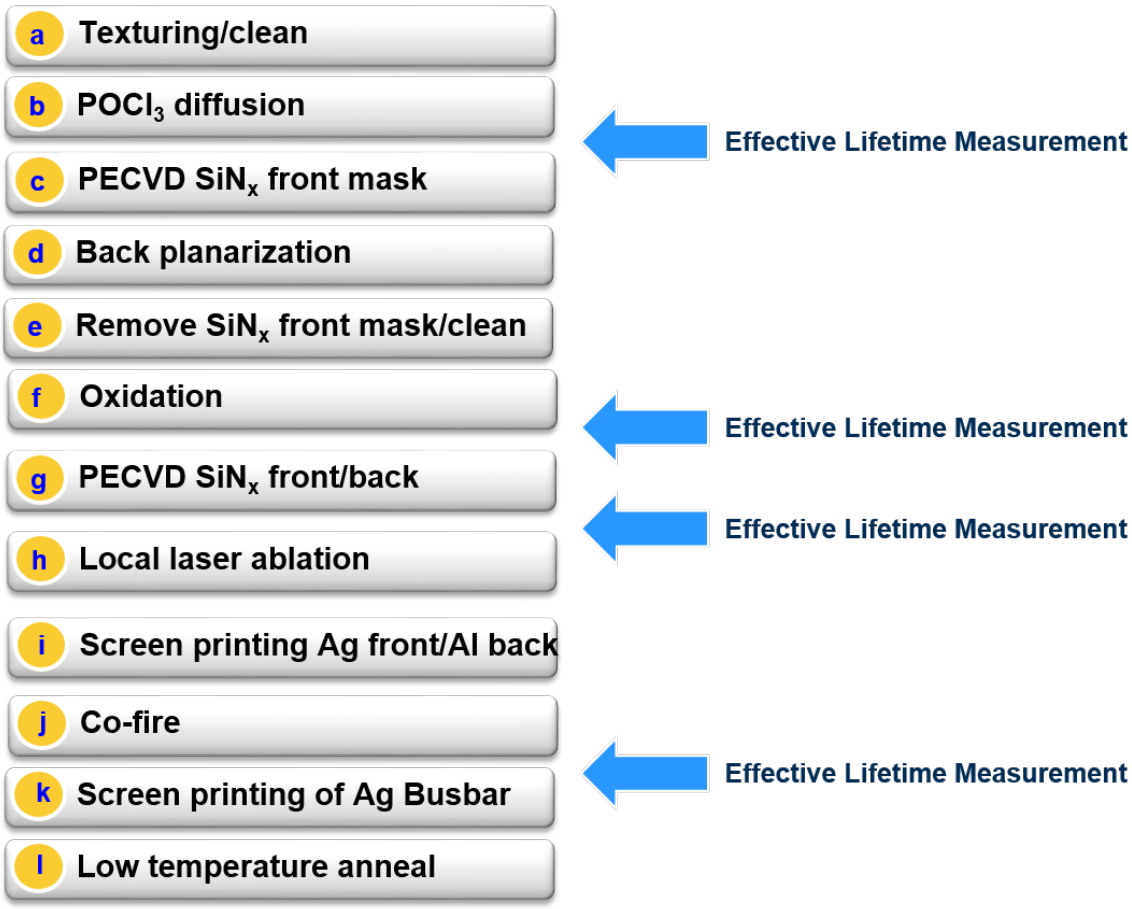



**Figure 75:** The process flow of screen-printed p-type PERC cells with $POCl_3$ diffused emitter, thin thermal $SiO_2/SiN_x$ passivation, and local Al BSF on the back.

Figure 75 shows the process flow used for p-type PERC cells which involved (a) random pyramid anisotropic texturing in a KOH based solution and clean, (b) $POCl_3$ diffusion, (c) a PECVD $SiN_x$ mask on the front, (d) single side rear planarization in a KOH based solution, (e) removal of front $SiN_x$ mask and clean, (f) thermal oxide passivation of both sides resulting in emitter sheet resistance of 75 Ω/sq on the front and 8 nm thick $SiO_2$ on the back, (g) PECVD $SiN_x$ deposition on front and back, (h) local laser opening through the rear dielectric stack to form ∼75 $\mu$m wide lines with 1 mm spacing, (i) screen printing of Ag grid on front with a commercial silver paste and Al paste on the entire back, (j) front and back contact firing in a belt furnace, (k) screen printing of floating busbar using a commercial low temperature Ag paste, and (l) low temperature anneal. The schematic of the PERC and PERT cell structure is shown in Figure 76 (a) and (b), respectively. The effective lifetime and Implied-$V_{oc}$ ($ImV_{oc}$) were measured using the Sinton Tester [114] at a minority carrier injection density of $10^{15}$ $cm^{-3}$ after the $POCl_3$ diffusion, thermal oxide passivation, PECVD $SiN_x$ coating and simulated contact firing without the metal contacts as indicated in Figure 75.

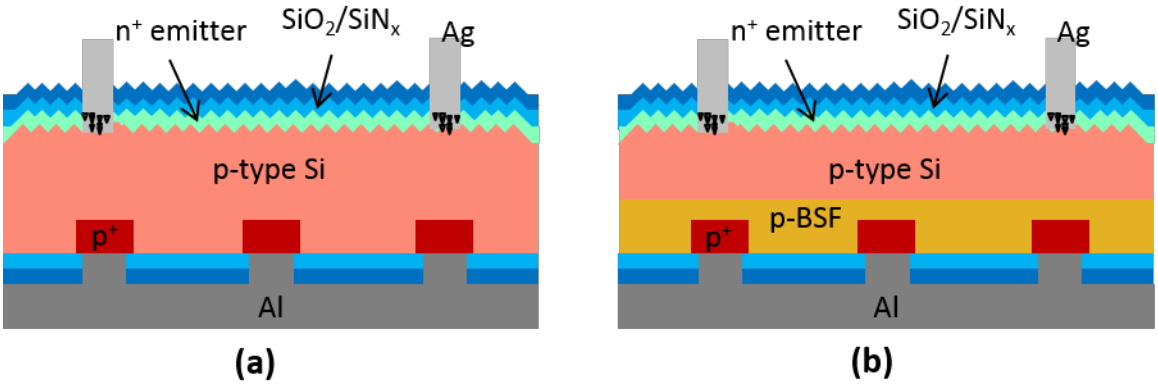



**Figure 76:** Schematic of the finished PERC cell (a) on Cz and epi-Si wafers and PERT cell (b) on epi-Si $pp^+$ wafer structure.

## 9.4 Results and Discussions

### 9.4.1 Effective Lifetime and Implied $V_{oc}$ of Cz and Epi-Si Wafers

Figures 77 and 78 show the effect of each key processing step on $ImV_{oc}$ and effective lifetime for the three materials used in this study: Cz wafer (Cz-p), Epi-Si wafer (Epi-p) and pp$^+$ Epi-Si substrate with in-situ p$^+$ BSF (Epi-pp$^+$). Note that the effective lifetime of the epi-Si wafers was slightly higher than the Cz material used in this study throughout the cell processing (Figure 78). After the final simulated firing step, the effective lifetime of the Epi-p wafer was 203 $\mu$s, compared to 144 $\mu$s for the Cz sample with about 6 mV higher $ImV_{oc}$ (Figure 77). Since all wafers were processed together, it is reasonable to assume that the front and back passivation quality is about the same and the difference in effective lifetime in Figure 78 is indicative of the difference in bulk lifetime. This is consistent with Powell et al. who reported high effective

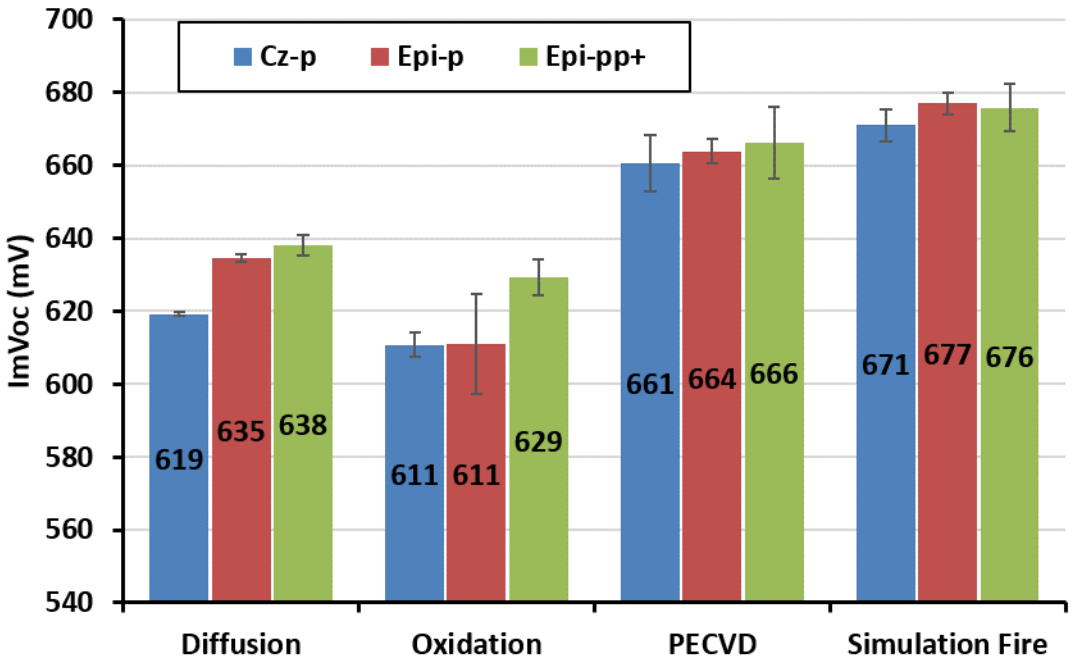



**Figure 77:** The measured implied $V_{oc}$ for the 3 groups of wafers (Cz-p, Epi-p, and Epi-pp$^+$) during the process sequence (diffusion, oxidation, PECVD and simulation fire).

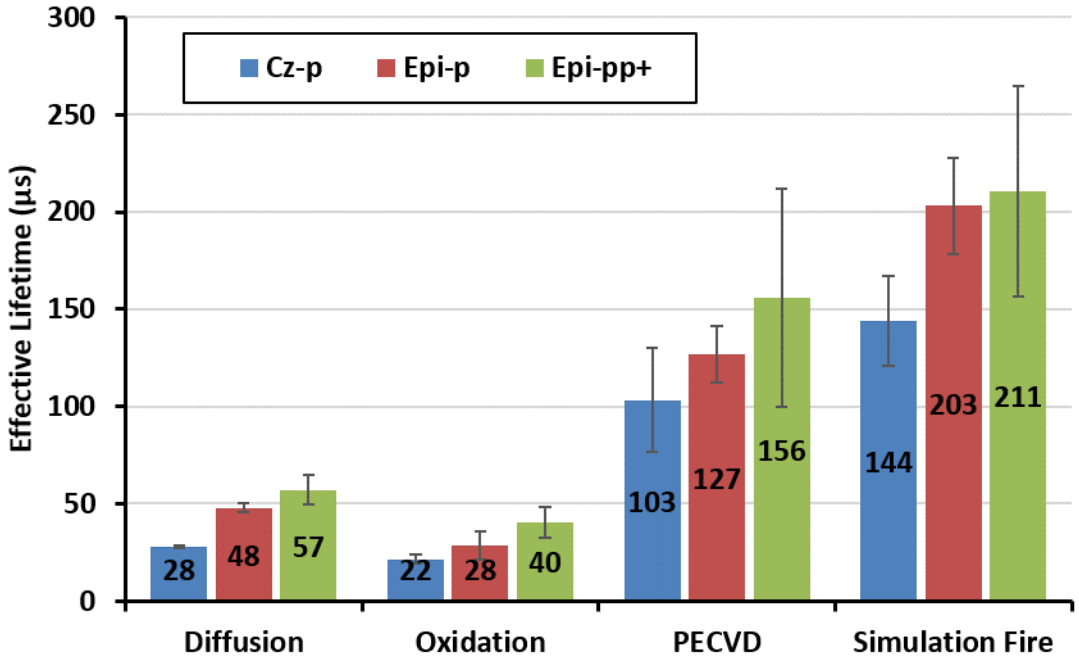



**Figure 78:** The measured effective lifetime for the 3 groups of wafers (Cz-p, Epi-p, and Epi-pp$^+$) during the process sequence (diffusion, oxidation, PECVD and simulation fire).

lifetime in epi-Si wafers after $POCl_3$ gettering and surface passivation [118]. Also notice that the effective lifetime and $ImV_{oc}$ were found to be very similar for the Epi-p and Epi-pp$^+$ wafers after the $SiN_x$ passivation and simulation firing.

### 9.4.2 Light IV Data of PERC and PERT Cells

Table 24 shows the measured Light IV data of the cells made on the three substrates in this experiment. The average efficiency of Cz PERC, epi-Si PERC and epi-Si PERT cells was 19.8%, 19.9% and 20.0%, respectively, with the best efficiency approaching 20.0%, 20.1% and 20.3%, respectively. In this study, efficiency of the epi-Si PERC cells was ~0.1% higher compared to the counterpart Cz PERC cells due to 2-3 mV higher $V_{oc}$. Note that efficiency improved by another ~0.2% when the epitaxial p$^+$ BSF layer was introduced. This is mainly because of the improvement in $FF$, which

is supported by the Sentaurus 2D Modeling discussed in Section 9.2. Although the cell efficiency improvement is within the standard deviation, the improvement in $FF$ is quiet clear since it is greater than the standard deviation of epi-Si PERC and PERT measured $FF$ (Table 24). The 20.3% large area screen-printed p-type PERT cell on epi-grown $pp^+$ wafer structure was certified by Fraunhofer CalLab. More recently, Q CELLS and Crystal Solar Inc. have demonstrated a 21.4% efficient screen-printed n-type epi-Si cell on epi-grown base material with built-in boron rear junction on the back [119].

**Table 24:** The LIV data calibrated to FhG CalLab for p-type PERC and PERT cell

| Cell Structure | ID | $V_{oc}$ (mV) | Isc (A) | $J_{sc}$ (mA /cm$^2$) | $FF$ (%) | Eff. (%) |
|---|---|---|---|---|---|---|
| Cz PERC | Best | 659 | 9.249 | 38.7 | 78.6 | 20.0 |
| Cz PERC | AVG of 7 | 657 | 9.177 | 38.4 | 78.5 | 19.8 |
| Cz PERC | STD of 7 | 4 | 0.069 | 0.3 | 0.5 | 0.2 |
| epi-Si PERC | Best | 662 | 9.263 | 38.5 | 78.7 | 20.1 |
| epi-Si PERC | AVG of 5 | 658 | 9.178 | 38.4 | 78.6 | 19.9 |
| epi-Si PERC | STD of 5 | 3 | 0.057 | 0.2 | 0.1 | 0.2 |
| epi-Si PERT | [1]Best | 662 | 9.272 | 38.5 | 79.4 | 20.3 |
| epi-Si PERT | AVG of 6 | 659 | 9.173 | 38.4 | 79.2 | 20.0 |
| epi-Si PERT | STD of 6 | 2 | 0.053 | 0.2 | 0.4 | 0.2 |

[1]LIV data is independently certified by Fraunhofer CalLab. N-factor, $R_s$ and Rsh data comes from our own measurement.

### 9.4.3 Understanding and Analysis of Internal Quantum Efficiency (IQE) Data of PERC and PERT cells with and without Light Bias

Figure 79 and 80 show the measured IQE data for the 3 types of cells with and without light bias, respectively. With light bias, all 3 cells gave good and comparable long wavelength IQE response. However, without the light bias, only the epi-Si PERT cell maintained good long wavelength response. The Cz and epi-Si PERC cells showed a degradation in the long wavelength IQE response without the light bias. This is attributed to the observed injection level dependence of $S_{eff}$ at the back surface (Figure 70) which can result from the combination of positive oxide charge

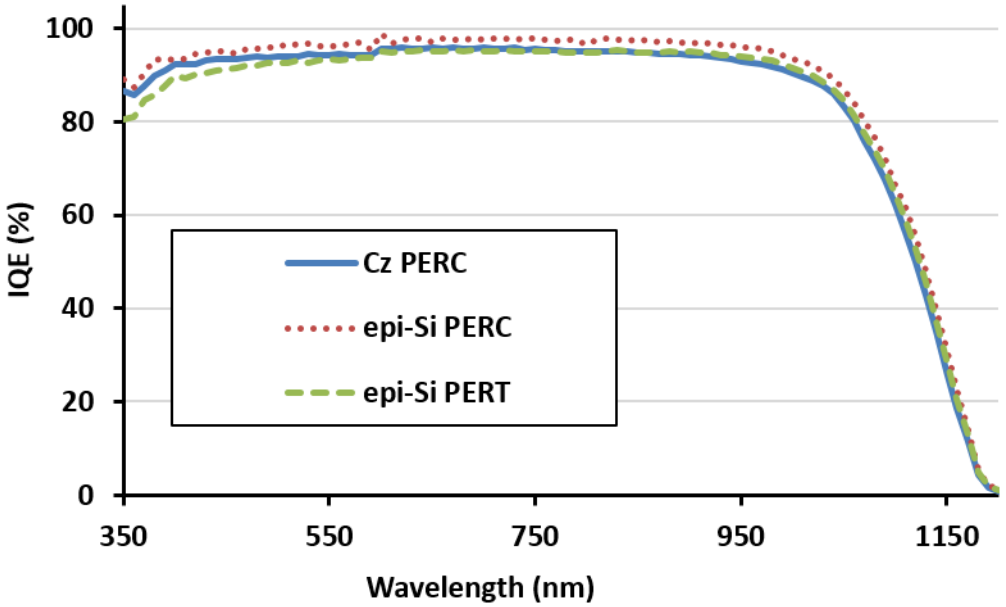



**Figure 79:** Measured IQE data for the Cz-p PERC, Epi-p PERC and Epi-pp$^+$ PERT cell with light bias.

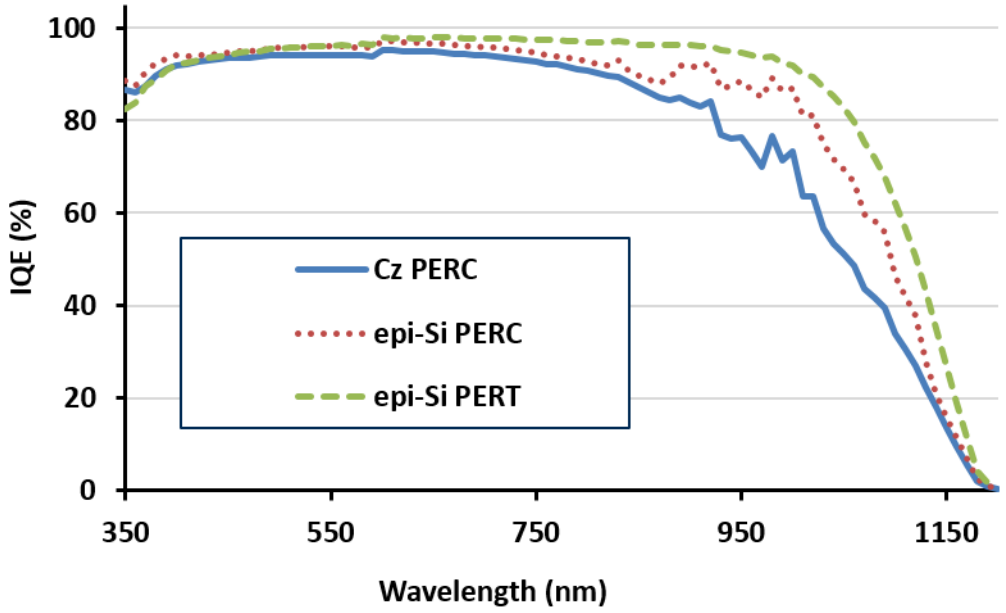



**Figure 80:** Measured IQE data for the Cz-p PERC, Epi-p PERC and Epi-pp$^+$ PERT cell without light bias.

and asymmetric $S_p/S_n$ ratio of <1 [111, 112]. In the PERT solar cell, because of the BSF, the back surface always remains in low level injection at one sun so $S_{eff} \approx S_n$ with or without light bias. The light bias independent long wavelength response in Figure 79 and 80 shows another benefit of PERT cell.

### 9.4.4 Photoluminescence Measurement of PERC and PERT Cells

Photoluminescence scan of the cell can reveal the recombination or defect map of the cell. Figure 81 (a)-(c) shows the Photoluminescence Image (PL) of the 3 groups of cells: Cz PERC, epi-Si PERC and epi-Si PERT. The mean PL response is about the same for the 3 cells. However, some defects (black dots) are observed in the epi-Si wafer. These may be stacking faults [54], as seen in the magnified microscope image (Figure 81 (d)). Even though few stacking faults are present, the average epi-Si material lifetime is good enough to give high $V_{oc}$ and efficiency.

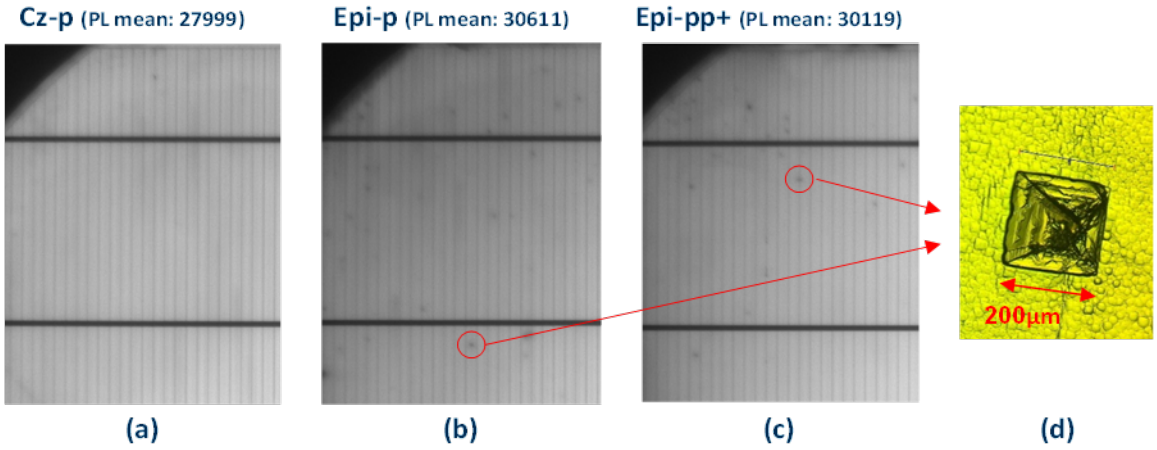



**Figure 81:** Photoluminescence Image for Cz PERC (a), epi-Si PERC (b), and epi-Si PERT (c) cells. The CCD microscope image for the stacking fault is shown in (d).

### 9.4.5 Comparison of Modeled and Experimental Light IV data for the PERC and PERT Cells

Table 25 again shows the comparison between the model (discussed in Section 9.2) and the experimental LIV data for PERC and PERT cells on epi-grown structures

(discussed in Section 9.4.2). Modeling predicted ∼0.5% higher efficiency for the PERT cell over the PERC structure. Experimentally, PERT cell efficiency was found to be ∼0.2% higher than the PERC cells. Slight reduction in the experimental efficiency enhancement is attributed to the difference in the back planarization process. In order to maintain the thickness of the $p^+$ layer, $pp^+$ wafer was etched only ∼5 $\mu$m during the back side planarization process as opposed to ∼20 $\mu$m removal for the PERC cells. This could lead to slightly inferior or incomplete back planarization in the PERT cells which could lead to higher n-factor and slightly lower $FF$ and efficiency, as observed in [120, 106]. Some difference between the modeled and experimental $V_{oc}$ can also come from the accuracy of $S_{eff}$ value used for lightly boron doped BSF surface from the literature [24, 23].

**Table 25:** The measured LIV data for p-type PERC and PERT cell using epi-Si material

| ID | Structure | $V_{oc}$ (mV) | $J_{sc}$ (mA /cm$^2$) | $FF$ (%) | Eff. (%) | n-factor | $R_s$ ($\Omega$-cm$^2$) |
|---|---|---|---|---|---|---|---|
| Modeled | PERC | 660 | 38.5 | 79.4 | 20.2 | 1.08 | 0.76 |
| Modeled | PERT | 667 | 38.7 | 80.4 | 20.7 | 1.02 | 0.70 |
| Experiment | PERC | 662 | 38.5 | 78.7 | 20.1 | 1.07 | 0.67 |
| Experiment | PERT | 662 | 38.5 | 79.4 | 20.3 | 1.07 | 0.51 |

## *9.5 P-type and N-type PERT Solar Cell with Epitaxially Grown Front and Back Built-in Doped Regions*

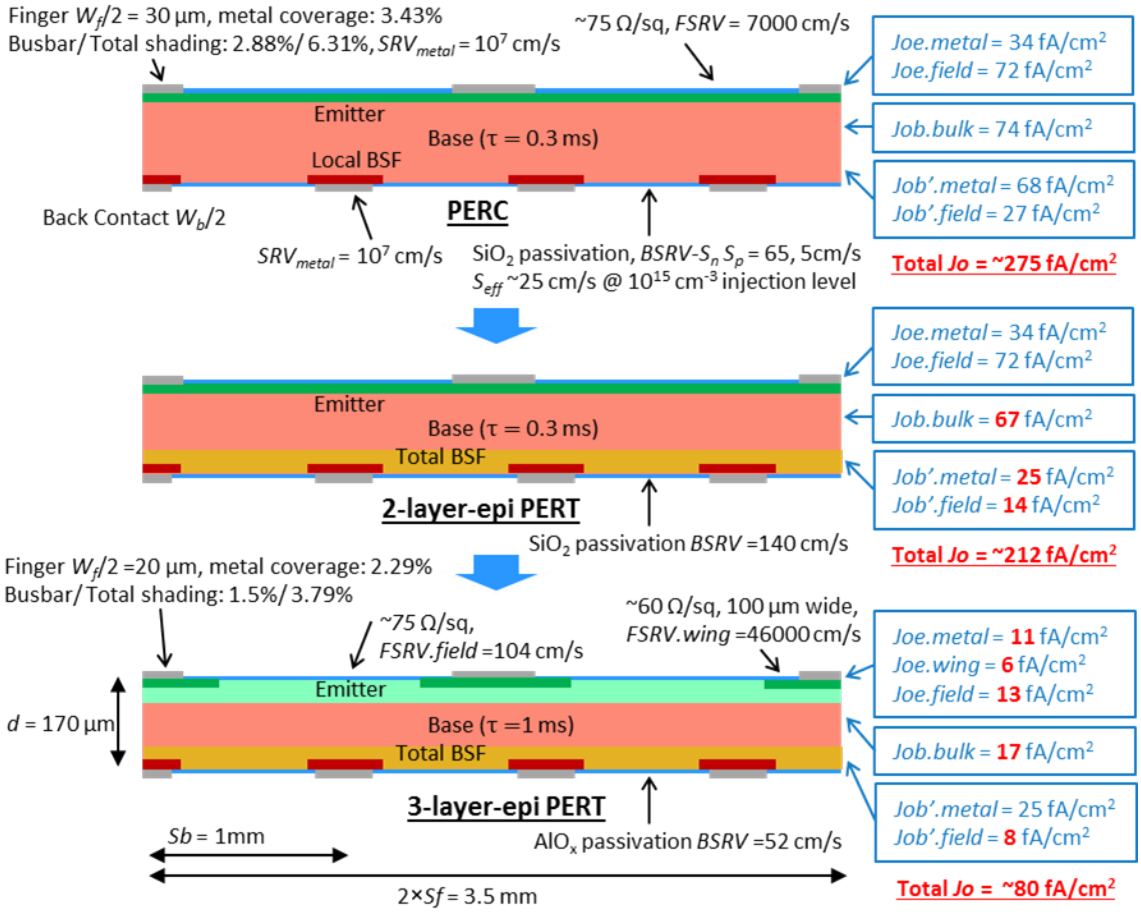
### 9.5.1 Modeling of p-type PERT Solar Cell with Epitaxially Grown Build-in Emitter and BSF

After demonstrating the efficiency enhancement of 2-layer-epi PERT on $pp^+$ epi-grown substrate by modeling and fabrication, we extended modeling to quantify the efficiency benefit of a PERT cell made from all three epi-grown layers (n-emitter, p-base, and $p^+$-BSF) shown in Figure 82. The modeled efficiency showed an efficiency

**Table 26:** The important Sentaurus-2D modeling parameters for the screen-printed 2-layer-epi and 3-layer-epi PERT

| Sentaurus Parameters | 20.7% 2-layer-epi PERT | 21.2% 3-layer-epi PERT | 22.7% 3-layer-epi PERT |
|---|---|---|---|
| $V_{oc}$ (mV) | 667 | 681 | 692 |
| $J_{sc}$ (mA/cm$^2$) | 38.7 | 38.7 | 39.7 |
| $FF$ (%) | 80.4 | 80.7 | 82.5 |
| Efficiency (%) | 20.7 | 21.2 | 22.7 |
| n-factor | 1.02 | 1.06 | 1.02 |
| Total $R_s$ ($\Omega$-cm$^2$) | 0.7 | 0.59 | 0.35 |
| Thickness $d$ ($\mu$m) | 170 | 170 | 170 |
| Front Contact Spacing $S_f$ (mm) | 1.75 | 1.75 | 1.75 |
| Front Contact Width $W_f$ ($\mu$m) | 60 (3.4%) | 60 (3.4%) | **40 (2.3%)** |
| Busbar Width (mm) | 0.9 (2.9%) | 0.9 (2.9%) | **0.5 (1.5%)** |
| Selective Emitter Width ($\mu$m) | N/A | **100** | 100 |
| Selective Emitter Profile | N/A | **Error, 0.85 $\mu$m** | Error, 0.85 $\mu$m |
| Selective Emitter $N_s$ (cm$^{-3}$) | N/A | **7.5×10$^{19}$** | 7.5×10$^{19}$ |
| Selective Emitter Sheet Resistance ($\Omega$/sq) | N/A | **60** | 60 |
| Emitter Profile | Measured, 0.45 $\mu$m | **Uniform, 5.5 $\mu$m** | Uniform, 5.5 $\mu$m |
| Emitter Surface Concentration (cm$^{-3}$) | 9×10$^{19}$ | **3×10$^{17}$** | 3×10$^{17}$ |
| Emitter Sheet Resistance ($\Omega$/sq) | ∼75 | ∼75 | ∼75 |
| Base Doping (cm$^{-3}$) | 8.6×10$^{15}$ | 8.6×10$^{15}$ | 8.6×10$^{15}$ |
| Base Resistivity ($\Omega$-cm) | 1.7 | 1.7 | 1.7 |
| Back Contact Spacing $S_b$ (mm) | 1 | 1 | 1 |
| Back Contact Width $W_b$ ($\mu$m) | 75 | 75 | 75 |
| Al Local BSF Profile | 5×10$^{18}$, 1.2 $\mu$m | 5×10$^{18}$, 1.2 $\mu$m | 5×10$^{18}$, 1.2 $\mu$m |
| Al Local BSF Width ($\mu$m) | 77.4 | 77.4 | 77.4 |
| Full BSF Profile | Uniform, 15 $\mu$m | Uniform, 15 $\mu$m | Uniform, 15 $\mu$m |
| Full BSF Doping (cm$^{-3}$) | 5×10$^{17}$ | 5×10$^{17}$ | 5×10$^{17}$ |
| Front Surface Recombination Velocity $FSRV$ (cm/s) | 7000 | **104** | 104 |
| $FSRV$ on n$^{++}$ selective emitter region (cm/s) | N/A | **4.6×10$^4$** | 4.6×10$^4$ |
| Contact Surface Recombination Velocity $SRV_{metal}$ (cm/s) | 10$^7$ | 10$^7$ | 10$^7$ |
| Lifetime $\tau$ ($\mu$s) | 300 | 300 | **1000** |
| Back Surface Recombination Velocity $BSRV$ (cm/s) | 140 | 140 | **52** |
| Back Contact Specific Contact Resistance (m$\Omega$-cm$^2$) | 2.6 | 2.6 | 2.6 |
| Series Resistance for Front Contact, Fingers and Busbars $R'_s$ ($\Omega$-cm$^2$) | 0.42 | 0.42 | **0.16** |

improvement from 20.7% to 22.7% with $V_{oc}$ increasing from 667 to 692 mV, $J_{sc}$ improving from 38.7 to 39.7 mA/cm$^2$, and $FF$ increasing from 80.4 to 82.5%. Six input parameters were changed in Table 26 to model the 3-layer-epi PERT cell compared to the modeling of the 2-layer-epi PERT cell in Section 9.2. Table 26 summarizes all the model input parameters and outputs for the 2-layer-epi and 3-layer-epi PERT




| Structure | Voc (mV) | Jsc (mA/cm²) | FF (%) | Eff. (%) | N-factor | Total $R_s$ (Ω-cm²) |
|---|---|---|---|---|---|---|
| PERC | 660 | 38.5 | 79.4 | 20.2 | 1.08 | 0.76 |
| 2-layer-epi PERT | 667 | 38.7 | 80.4 | 20.7 | 1.02 | 0.70 |
| 3-layer-epi PERT | 692 | 39.7 | 82.5 | 22.7 | 1.02 | 0.35 |

**Figure 82:** From 2-layer-epi PERT to 3-layer-epi PERT. The cross-section of the unit cell of both 2-layer-epi and 3-layer-epi PERT used in Sentaurus 2D modeling were shown along with the important input parameters, LIV outputs, and $J_o$ components. The starting PERC cell is also shown here for comparison.

cells.

(1). The field emitter design was changed from the $POCl_3$ diffused ~75 Ω/sq profile to a 5.5 $\mu$m deep n-type uniform epi-grown profile with $3\times10^{17}$ $cm^{-3}$ doping concentration and sheet resistance of ~75 Ω/sq. Similar sheet resistance of $POCl_3$ and epi-grown emitters were chosen in order to have better comparison in cell performance with the same finger spacing, as shown in Figure 82 and 84. Based on [21], $FSRV$ of 104 cm/s was used for $3\times10^{17}$ $cm^{-3}$ phosphorus surface passivated by $SiO_2$ as shown in Figure 83. Model calculations in Figure 85 revealed that $J_{oe}$ of this epi-grown emitter is superior ($14 \times 97.7\% = 13$ $fA/cm^2$) to $POCl_3$ emitter ($74 \times 97.7\% = 72$ $fA/cm^2$).

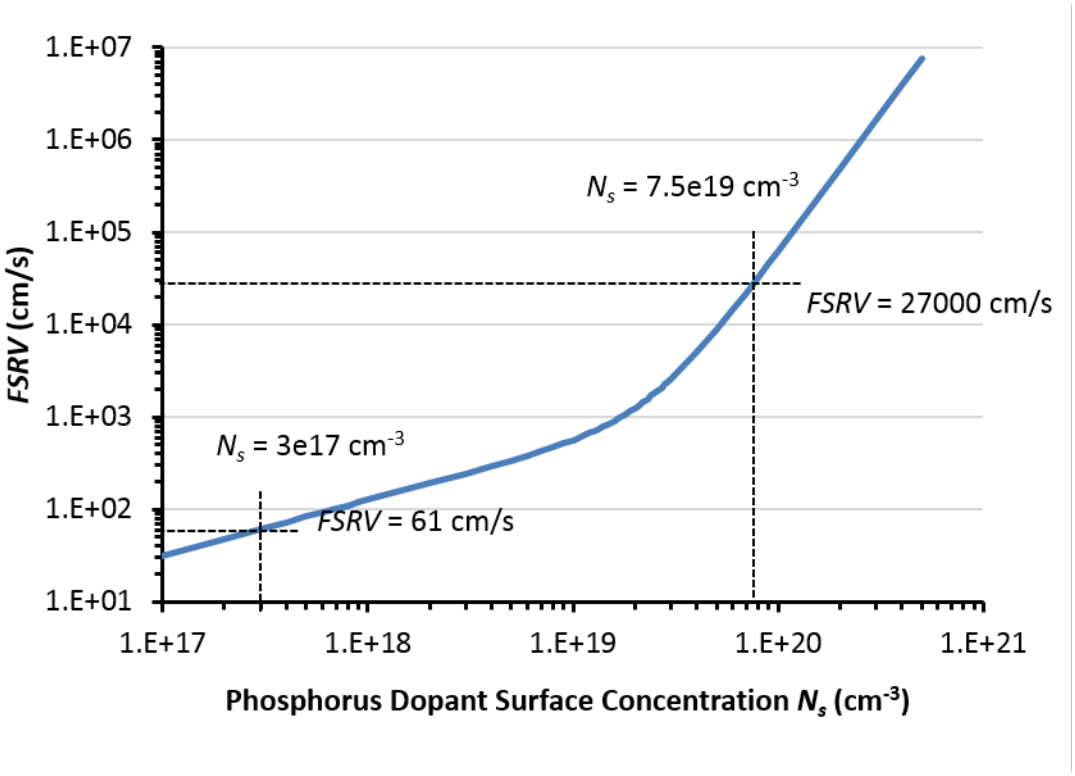



**Figure 83:** Extracted $FSRV$ as a function of phosphorus surface concentration pssivated by $SiO_2$ on planar surface [21]. We used a texture multiplier of 1.7 for texture surface.

(2). Since it is difficult to make ohmic contact to epi-grown emitter with surface concentration of $3\times10^{17}$ $cm^{-3}$, a selective emitter was implemented with heavy doping

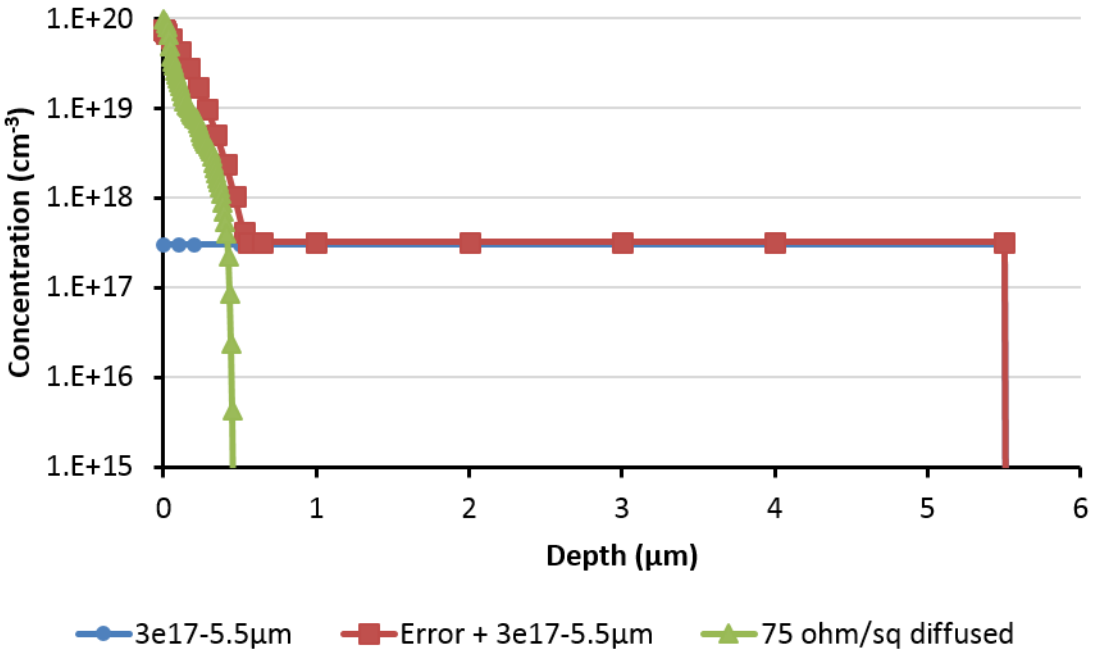



**Figure 84:** Emitter profiles for uniform epi-grown field emitter (3e17-5.5$\mu$m), diffused/implant emitter on top of the uniform epi-grwon emitter underneath the contact(Error + 3e17-5.5$\mu$m), and diffused emitter (75 ohm/sq diffused).

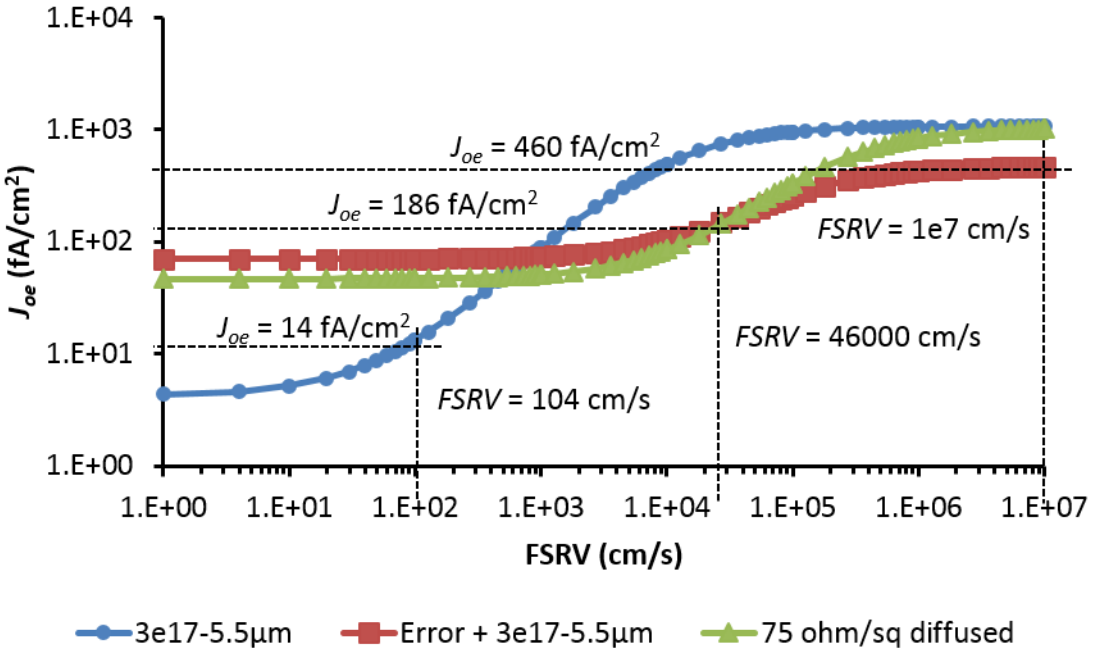



**Figure 85:** Modeled $J_{oe}$ vs $FSRV$ curve for uniform epi-grown field emitter (3e17-5.5$\mu$m), diffused/implant emitter on top of the uniform epi-grwon emitter underneath the contact(Error + 3e17-5.5$\mu$m), and diffused emitter (75 ohm/sq diffused).

($n^{++}$) under the contacts. An error function $n^{++}$ profile with $7.5\times10^{19}$ $cm^{-3}$ surface concentration and $\sim$ 0.85 $\mu$m depth was used in modeling. Since screen-printed contact width is $\sim$40 $\mu$m while the width of $n^{++}$ is 100 $\mu$m, there is 60 $\mu$m wind width or region between metal contact and edge of $n^{++}$ region. This selective emitter region has a sheet resistance of $\sim$60 $\Omega$/sq on p-type base as shown in Figure 82 and 84. Using the data in Figure 83 [21], an $FSRV$ of 46000 cm/s was used for $7.5\times10^{19}$ $cm^{-3}$ phosphorus doped surface passivated by $SiO_2$. Model calculations in Figure 85 showed that heavy doping under the metal reduced $J_{oe.metal}$ from 34 fA/cm$^2$ ($1000 \times 3.4\% = 34$ fA/cm$^2$ for 2-layer-epi PERT) to 17 fA/cm$^2$ (3-layer-epi PERT). The 17 fA/cm$^2$ is the sum of $J_{oe.metal}$ ($460 \times 2.3\% = 11$ fA/cm$^2$) and $J_{oe.wing}$ ($186 \times 3.4\% = 6$ fA/cm$^2$) for the 3-layer-epi PERT cell.

(3). Thinner finger width of 40 $\mu$m (2.29% front metal coverage) was used for the 3-layer-epi PERT compared to 60 $\mu$m wide fingers (3.43% front metal coverage) in the 2-layer-epi PERT. The $R'_s$ was calculated to be 0.16 $\Omega$-cm$^2$ using equations (57) -(60) and measured/projected paste parameters (Table 27).

**Table 27:** Measured and Projected Screen-Printed Contact Parameters

| Parameters | Values |
|---|---|
| Effective Finger Length $a$ (cm) | 1.5 |
| Busbar Length $b$ (cm) | 15 |
| IV Tester Probes Spacing $c$ (cm) | 1 |
| Finger Width $W_f$ ($\mu$m) | [1]40 |
| Spacing (mm) | 1.75 |
| Busbar Resistance $R_{bus\_m}$ ($\Omega$) | 0.03 |
| Finger Line Resistance $R_{fl\_m}$ ($\Omega$/cm) | 0.49 |
| Specific Contact Resistance $R_{fc\_m}$ ($\Omega$-cm$^2$) | 2.2 |
| $R_{s\_bus}$ ($\Omega$-cm$^2$) | 0.00 |
| $R_{s\_fin}$ ($\Omega$-cm$^2$) | 0.06 |
| $R_{s\_fc}$ ($\Omega$-cm$^2$) | 0.10 |
| $R'_s$ ($\Omega$-cm$^2$) | 0.16 |

[1]projected 40 $\mu$m finger width in the near future. Today measured finger width was close to 50 $\mu$m.

$$R_{s\_bus} = \frac{1}{3} \cdot a \cdot \left(\frac{c}{2}\right)^2 \cdot \frac{R_{bus\_m}}{b} \tag{57}$$

$$R_{s\_fin} = \frac{1}{3} \cdot a^2 \cdot spacing \cdot R_{fl\_m} \tag{58}$$

$$R_{s\_fc} = \frac{R_{fc\_m}}{W_f} \cdot spacing \tag{59}$$

$$R'_s = R_{s\_bus} + R_{s\_fin} + R_{s\_fc} \tag{60}$$

(4). Busbar width of 0.5 mm (1.5% busbar shading) was used in the 3-layer-epi PERT compared to 0.9 mm (2.88% busbar shading) in 2-layer-epi PERT.

(5). Higher bulk lifetime of 1 ms in the 3-layer-epi PERT cell was used compared to 0.3 ms in the 2-layer-epi PERT. This reduces $J_{ob.bulk}$ from 67 to 17 fA/cm$^2$ using following equation (61).

$$J_{ob.bulk} = qW \frac{n_i^2}{\tau_n N_A} \tag{61}$$

(6). A $BSRV$ of 52 cm/s on top of the $5\times10^{17}$ boron doped back surface was used. This was estimated from Heox's data [24] in Figure 86 for the $Al_2O_3$ passivated $5\times10^{17}$ boron doped surface. This is much lower than the $S_{eff}$ of 270 cm/s for oxide passivated BSF in the 2-layer-epi PERT. Model calculations in Figure 88 shows that this reduces this reduces $J'_{ob.field}$ from $15\times92.5\% = 14$ to $9 \times 92.5\% = 8$ fA/cm$^2$. The different BSF profiles for the 3-layer-PERT cell is also shown in Figure 87 with local BSF from PERC for comparison.

### 9.5.2 Proposed Process Flow for P-type Front Junction PERT and N-Type Back Junction PERT with Epitaxially Grown Front and Back Doping Regions

The process flow for the 3-layer-epi PERT is proposed and shown in Figure 89. The epi-grown 3-layer-epi wafer structure consists of $n^+$ emitter layer, p-type base layer, and $p^+$ BSF layer. By applying the process flow shown in Figure 89, the p-type front junction 3-layer-epi PERT solar cell can be finished. Note that this process is very similar to the industrial p-type PERC screen printing process as described in Section 8.1 and 9.3. The main difference is that instead of the formation of a homogeneous phosphorus doped emitter, selectively doped region is formed for the contact. Also

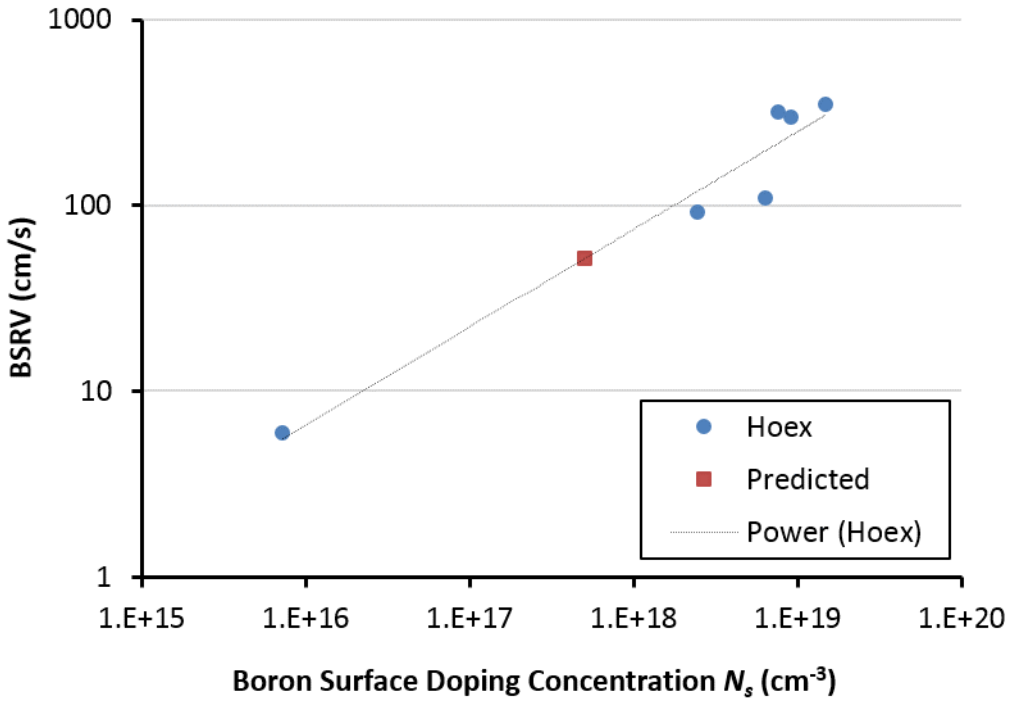



**Figure 86:** Extracted and predicted $FSRV$ data as function of Boron doped surface passivated by $AlO_x$ [24].

note that, if we can now change the p-type base into n-type, a n-type back junction 3-layer-epi PERT solar cell can be finished by using identical process (Figure 89). Some advantages for n-type over p-type material include more tolerance to impurities [105], higher bulk lifetime, and no light-induced degradation from boron-oxygen complex [121].

### 9.5.3 Sentaurus Modeling to Quantify the Impact of Base Resistivity and Lifetime on P-type Front Junction PERT and N-Type Back Junction PERT cells

We extended our model to calculate the LIV data for the p-type front junction PERT and n-type back junction PERT solar cells with different base resistivity and bulk lifetime. The results are shown in Figures 90 and 91. According to the model calculation, >22.7% efficiency can be achieved with both cell structures. For p-type front junction PERT, lifetime >1 ms and resistivity of 1-2 Ω-cm are required (Figure 90),

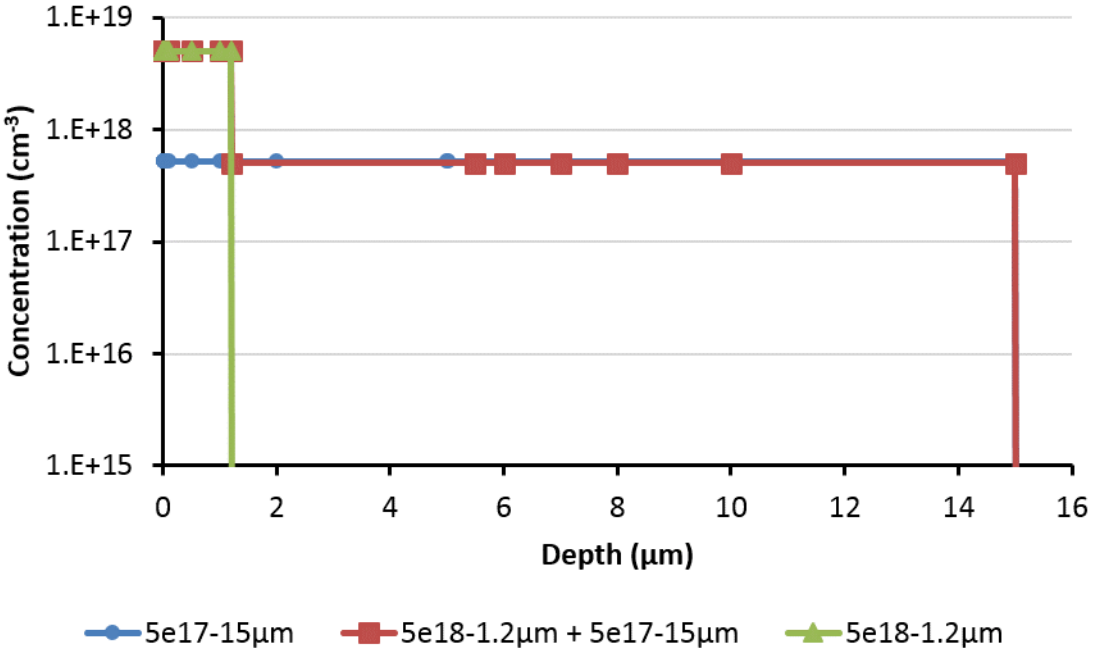



**Figure 87:** BSF profiles for uniform epi-grown BSF (5e17-15$\mu$m), Al local BSF on top of the uniform epi-grwon BSF underneath the contact(5e18-1.2$\mu$m + 5e17-5$\mu$m), and Al local BSF (5e18-1.2$\mu$m).

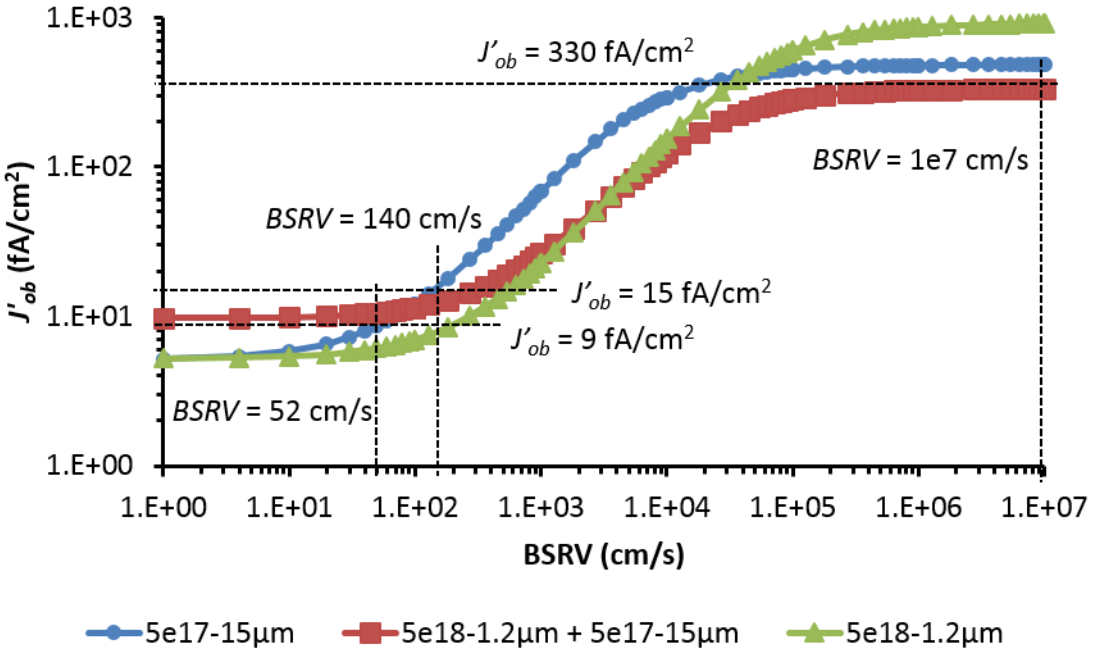



**Figure 88:** Modeled $J'_{ob}$ vs $BSRV$ curve for uniform epi-grown BSF (5e17-15$\mu$m), Al local BSF on top of the uniform epi-grwon BSF underneath the contact(5e18-1.2$\mu$m + 5e17-5$\mu$m), and Al local BSF (5e18-1.2$\mu$m).

while n-type back junction PERT cell needs lifetime >3 ms and resistivity of 5-10 Ω-cm (Figure 91).

### 9.5.4 Sentaurus Modeling to Assess the Impact of the Thickness of Front Epi-grown Phos-doped layer on the Performance of P-type Front Junction PERT and N-Type Back Junction PERT Cells

Finally, we modeled the effect of the thickness of the front phosphorous doped epi-grown region for both the p-type front junction and n-type back junction PERT solar cells. The base materials were chosen to be 1.7 Ω-cm and 1 ms for p-PERT, and 10

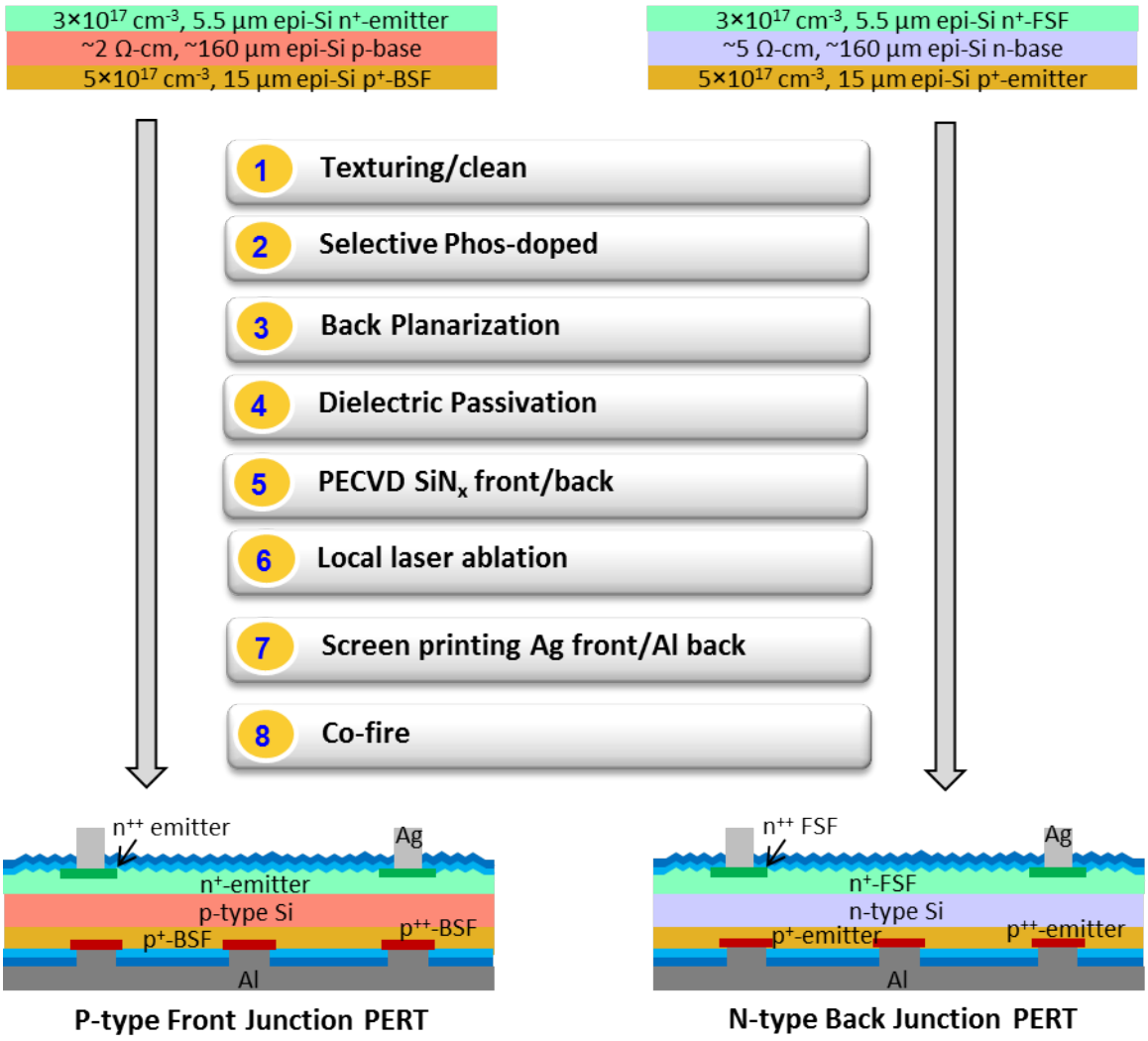



**Figure 89:** Proposed process flow of the p-type front junction PERT and n-type back junction PERT from 3-layer-epi Si wafer structure.

Ω-cm and 3 ms for n-PERT with all the other input parameters listed in Table 26, column called "22.7% 3-layer-epi PERT". Figure 92 shows that 4-7 $\mu$m epi-grown phosphorous doped region is needed for p-type front junction cell to achieve the highest efficiency of 22.7%, while 2-6 $\mu$m for n-type back junction cell can achieve the highest efficiency of 22.7%. The efficiency plateau is important, since the epi-Si wafer structure are first grown and then textured in the proposed process flow (Figure 89). The plateau relaxes wafer texturing requirements since textured pyramid size is generally 3-5 $\mu$m. Comparison of Figures 74 and 92 shows that the $n^+$-epi is more critical for front junction cell because more carriers are generated in the front than the back of a solar cell. The Auger recombination limited lifetime was used in the lightly doped regions for the modeling, where the auger limited lifetime is ~34 $\mu$s in the $5\times10^{17}$ $cm^{-3}$ boron doped region and ~44 $\mu$s in the $3\times10^{17}$ $cm^{-3}$ phosphorus doped region.

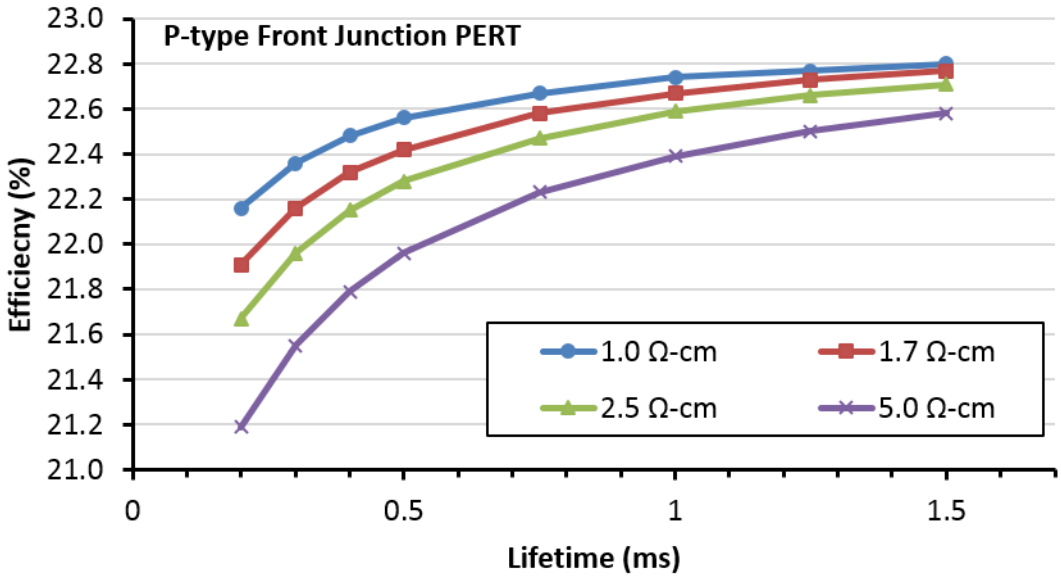



**Figure 90:** P-type front junction PERT cell efficiency as function of lifetime and resistivity by using Sentaurus 2D modeling.

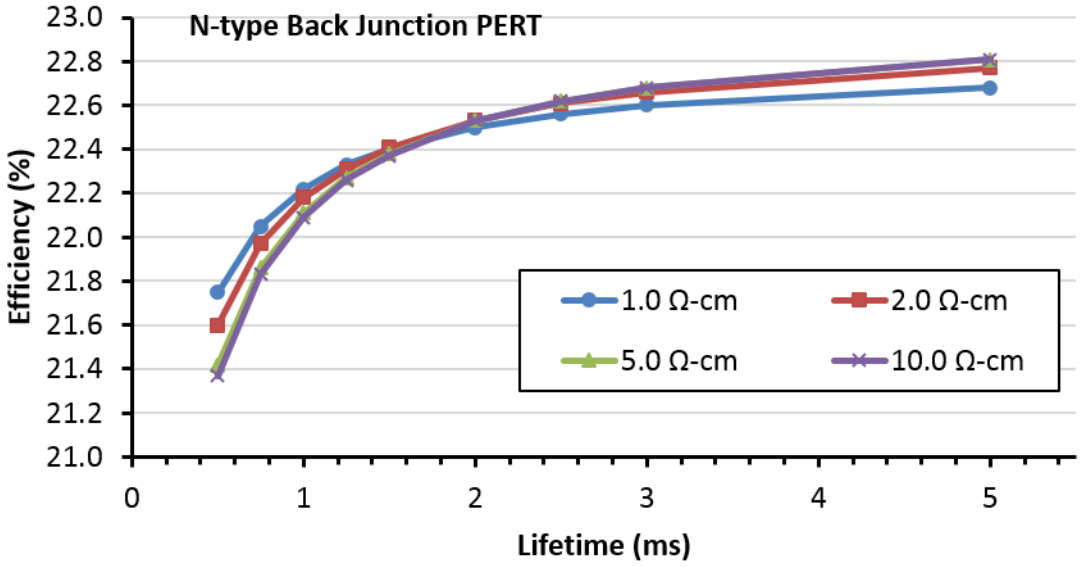



**Figure 91:** N-type back junction PERT cell efficiency as function of lifetime and resistivity by using Sentaurus 2D modeling.

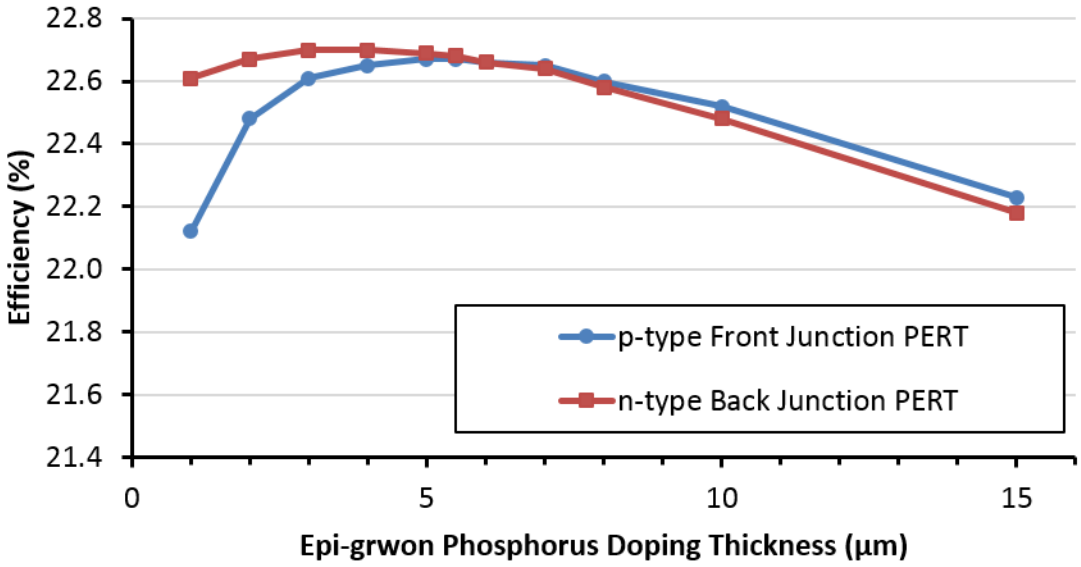



**Figure 92:** Front and Back junction PERT cell efficiency as function of different front phosphorus doping thickness using Sentaurus 2D modeling.

## *9.6 Summary*

In this task, the potential of epi-Si material and epi-grown structures for high efficiency cell is studied. Sentaurus 2D model was used to study the cell performance

as a function of different BSF profiles in p-PERT solar cells. The model showed that the BSF needs to be carefully chosen in order to realize the full efficiency advantage over the counterpart PERC cells. With identical front, p-type PERT solar cell with a lightly doped thick boron BSF (15-30 $\mu$m, $10^{17}$-$10^{18}$ cm$^{-3}$) can give efficiency enhancement of $\sim$0.5% over the PERC cell because of higher $FF$. If the BSF doping is too high, then the loss in $V_{oc}$ and $J_{sc}$ due to recombination in the BSF can offset the gain in $FF$ and result in lower performance. Following the model prediction, p-type PERT cells were fabricated on epi-grown pp$^+$ substrates with in-situ lightly doped thick BSF. Using identical process, PERC cells were also fabricated on p-type epi-Si and Cz wafers for comparison. Greater than 20% cells were achieved for all these devices with epi-Si PERT cell giving the highest efficiency of 20.3%. This was 0.2-0.3% higher than the PERC cells on epi-Si and Cz wafers. Finally, the potential of a three layer (emitter, base and BSF) epi-grown PERT solar cell was modeled, which showed >22.7% efficiency is achievable by obtaining the right combination of base lifetime and resistivity using more advanced screen-printed technology (40 $\mu$m wide finger and 1.5% narrow busbar shading).

# CHAPTER X

# TASK 6: MODELING THE POTENTIAL OF NEXT GENERATION SCREEN-PRINTED N-TYPE FRONT JUNCTION CZ SI SOLAR CELLS WITH TUNNEL OXIDE PASSIVATED BACK CONTACT

In order to achieve the highest cell efficiency, the recombination loss in the entire cell needs to be minimized. Current industry cell performance is largely limited by the recombination in metal, surface and doped regions. Carrier selective passivated contact composed of tunnel oxide, $n^+$ polycrystalline Si (Poly-Si) and metal on top of a n-Si absorber (Figure 93) can significantly lower the recombination current density ($\leq$8 fA/cm$^2$) under the contact since metal and doped regions are not in direct contact with the absorber. In addition, such a contact on the rear side of an n-Si allows majority carriers (electrons) to tunnel easily but blocks the minority carriers (holes) effectively, which provides excellent specific contact resistance (5-10 m$\Omega$-cm$^2$). Using this concept, a joint program between GT (Georgia Institute of Technology), Fraunhofer ISE (Fraunhofer Institute for Solar Energy System ISE), and NREL (National Renewable Energy Laboratory) has produced 24.9% efficiency on a small area (4 cm$^2$) laboratory cell (Figure 94 a) on Fz Si with photolithography front contacts [13]. This task shows a methodology and modeling of this 24.9% efficient cell using the Santaurus 2D device model, which involves replacing the TOPCon region on the back by carrier selective electron and hole recombination velocities to match the measured dark saturation current density ($J'_{ob}$) of the TOPCon region as well as all the light IV parameters of the TOPCon cell. The modeling is then extended to assess

the efficiency potential of large area TOPCon cell on commercial grade n-type Cz material with conventional screen-printed front contact with boron doped emitter on front and TOPCon back. To use realistic input parameters for the base and emitter of the TOPCon Cz cell, a 21% n-type PERT cell (Figure 98 a) was fabricated with 90 Ω/sq homogenous emitter and 5 Ω-cm 1.5 ms lifetime base. Device modeling showed that if the back of this cell is replaced by the above TOPCon structure with $J'_{ob}$ ≤8 fA/cm$^2$, the cell efficiency will improve to only ∼21.6% because the performance is limited by the high emitter saturation current density $J_{oe}$ =150 fA/cm$^2$. Modeling also showed that the implementation of a selective emitter (150/20 Ω/sq) on the front can raise the efficiency of TOPCon Cz cell to ∼22.6%. Finally, it is shown that screen

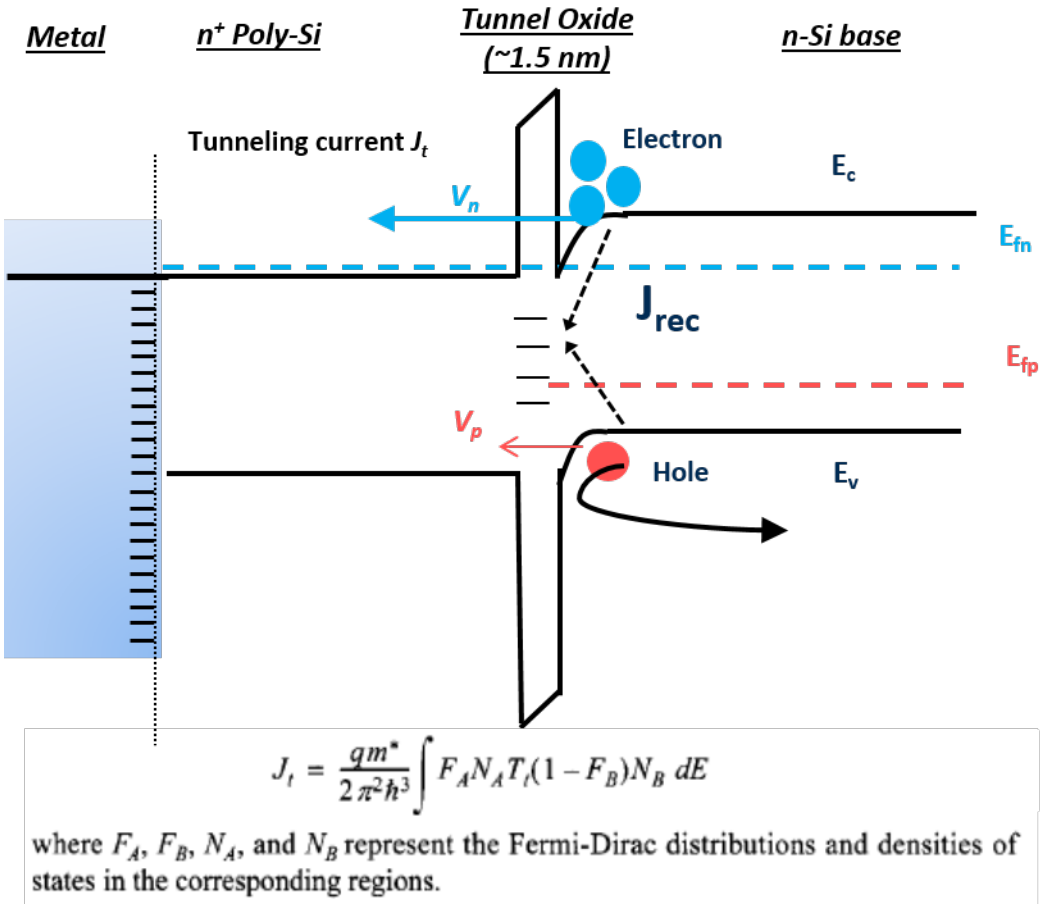



**Figure 93:** Band diagram of the metal/ n$^+$ Poly-Si/ tunnel oxide/ n-base passivated contact system.

printing of 40 $\mu$m wide lines (~5.5% shadow loss) in combination with floating busbar on the front and improved bulk material quality (10 Ω-cm, 3 ms lifetime) can raise the single side TOPCon Cz cell efficiency to 23.2%.

## *10.1 Modeling of 24.9% TOPCon Cell with Photolighography Contact*

Sentaurus Model was used in this study to match the 24.9% photolithography front contact TOPCon cell fabricated by Fraunhofer ISE [13]. The physical models recommended by Pietro P. Altermatt [28] were chosen for the device modeling, including Fermi-Dirac Statistics, Klaassens unified mobility model, Schenk bandgap narrowing model and Auger recombination coefficient from Dziewior and Schmid.

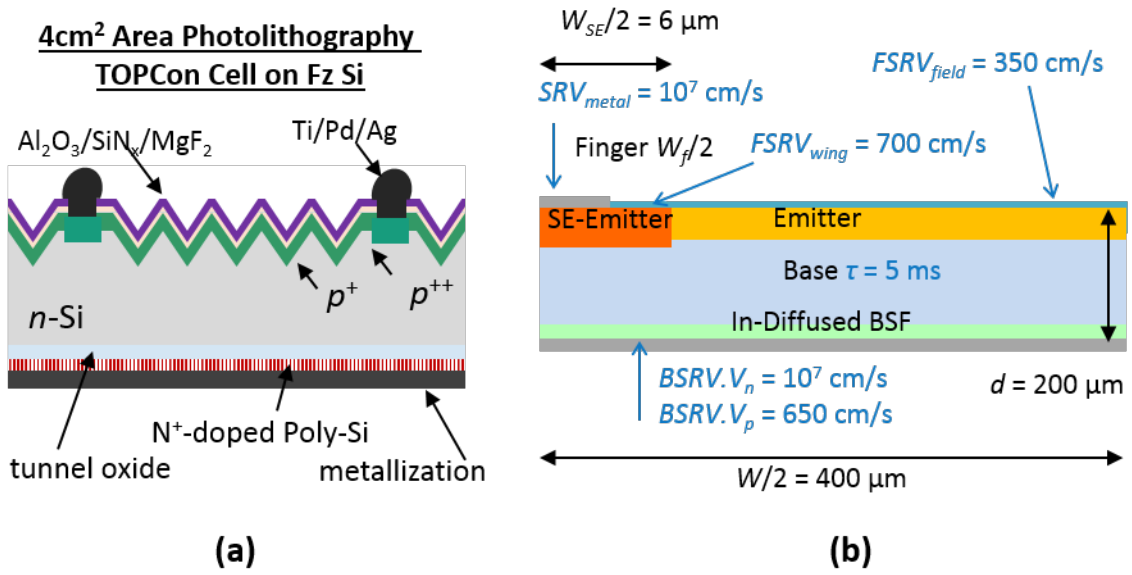



**Figure 94:** (a) Schematic diagram of the 24.9% photolithagraphy TOPCon cell. Figure courtesy Fraunhofer ISE. (b) The cross-section schematic scheme of the 24.9% photolithagraphy TOPCon solar cell for Sentaurus 2D Modeling.

First step of this modeling involves building the appropriate unit cell, cross section of which is shown in Figure 94 (b). All the required input parameters (measured and extracted) for the base, emitter and front contact regions are listed in Table 28.

For the simulation of the passivated rear TOPCon contact, different models can

**Table 28:** Important Input Parameters for Sentaurus 2D Device Model of 24.9% Photolithography TOPCon Cell

| Sentaurus Parameters | PL contact TOPCon |
|---|---|
| Effective Front Finger Width $W_f$ ($\mu$m) | 8.8 (1.1%) |
| Front Shading Width ($\mu$m) | [1]20 (2.5%) |
| Front Finger Spacing $W$ (mm) | 0.8 |
| Thickness ($\mu$m) | 200 |
| Field Emitter Profile | Measured |
| Field Emitter Sheet Resistance ($\Omega$/sq) | $\sim$150 |
| Field Emitter Surface Concentration (cm$^{-3}$) | $4.8\times10^{18}$ |
| Field Emitter Junction Depth ($\mu$m) | $\sim$1.65 |
| Selective Emitter Profile | Measured |
| Selective Emitter Sheet Resistance ($\Omega$/sq) | $\sim$20 |
| Selective Emitter Surface Concentration (cm$^{-3}$) | $\sim3\times10^{19}$ |
| Selective Emitter Junction Depth ($\mu$m) | $\sim$3 |
| Selective Emitter Junction Width $W_{SE}$ ($\mu$m) | 12 |
| Substrate Doping (cm$^{-3}$) | $5\times10^{15}$ |
| Substrate Resistivity ($\Omega$-cm) | 1 |
| Field FSRV $FSRV_{field}$ (cm/s) | 350 |
| Wing FSRV $FSRV_{wing}$ (cm/s) | 700 |
| Front Contact FSRV $SRV_{metal}$ (cm/s) | $10^7$ |
| Lifetime $\tau$ (ms) | 5 |
| Back Specific Contact Resistance (m$\Omega$-cm$^2$) | 5 |
| Series Resistance for Front Contact, Fingers and Busbars ($\Omega$-cm$^2$) | 0.21 |
| Measured $J'_{ob}$ (fA/cm$^2$) | 8 |
| Back Contact Electron SRV $BSRV.v_n$ (cm/s) | [2]$10^7$ |
| Back Contact Hole SRV at n Si/ n$^+$ Si interface $BSRV.v_p$ (cm/s) | 3.5 |
| In-Diffused Back Surface Field Profile | Measured |
| Back Contact Hole SRV at n$^+$ Si/ tunnel oxide interface $BSRV.v_{p-n^+ox}$ (cm/s) | 650 |

[1]Finger shading $\sim$2% and busbar shading $\sim$0.5%. [2]Model efficiency actually stayed the same with $BSRV.v_n$ in the range of $10^4$-$10^7$ cm/s.

be used. Steinkemper et al. used a nonlocal tunneling model to simulated the carrier transport [122]. Peibst et al. however used a micro holes in the oxide to describe the carrier transport for such oxide passivated contact structures [123]. In this paper, we are using a simple contact model replacing the carrier selective TOPCon region by

highly asymmetric electron and hole velocities ($v_n$ and $v_p$, respectively) with corresponding current densities of

$$J_n = qv_n(n - n_0) \tag{62}$$

$$J_p = qv_p(p - p_0) \tag{63}$$

Note that our modeling does not incorporate exact tunneling mechanism and parameters but its carrier selective behavior is captured in the highly asymmetric values of $v_n$ and $v_p$. Therefore, we need to have fairly accurate assessment of $v_n$ and $v_p$. Since electrons can tunnel quite easily through the oxide (band diagram in Figure 93), we assumed $v_n = 10^7$ cm/s. This is also supported by very low specific contact resistance ($\sim$5 m$\Omega$/cm$^2$) of the TOPCon structure as measured by TLM method [13]. We have also found that $v_n$ in the range of $10^4$ to $10^7$ cm/s has virtually no impact on efficiency and light IV parameters (Figure 95). Note that this TOPCon model set-up does predict asymmetrical values of $v_n$ and $v_p$ or good carrier selectivity is essential for the solar cell as also described in [124].

However, accurate determination of the hole velocity ($v_p$) is very critical, which is a function of carrier selectivity as well as interface recombination. Since at this time all the input parameters are known except for $v_p$, we applied the Sentaurus model to generate a $J'_{ob}$ versus $v_p$ curve for the device. This is done by first making $v_p = 0$ cm/s and running the Sentaurus model to obtain cell IV parameters. Then the total $J_{o1}$ is calculated from $V_{oc}$ and $J_{sc}$ ($V_{oc} = \frac{kT}{q} ln \frac{J_{sc}}{J_o}$ ). This corresponds to an ideal TOPCon structure with no recombination below the base ($v_p = 0$) and the calculated $J_{o1}$ represents total recombination above the TOPCon region including base, emitter and front contacts. Next, $v_p$ value is varied in the range of 0 to $10^4$ cm/s and total $J_o$ is calculated from $V_{oc}$ and $J_{sc}$ obtained from Sentaurus model for each value of $v_p$. The difference between $J_o$ and $J_{o1}$ corresponds to $J'_{ob}$ or recombination associated with the TOPCon region alone since no change is made to the parameters above the tunnel oxide. This concept and approach resulted in a plot of $J'_{ob}$ vs $v_p$, shown by the

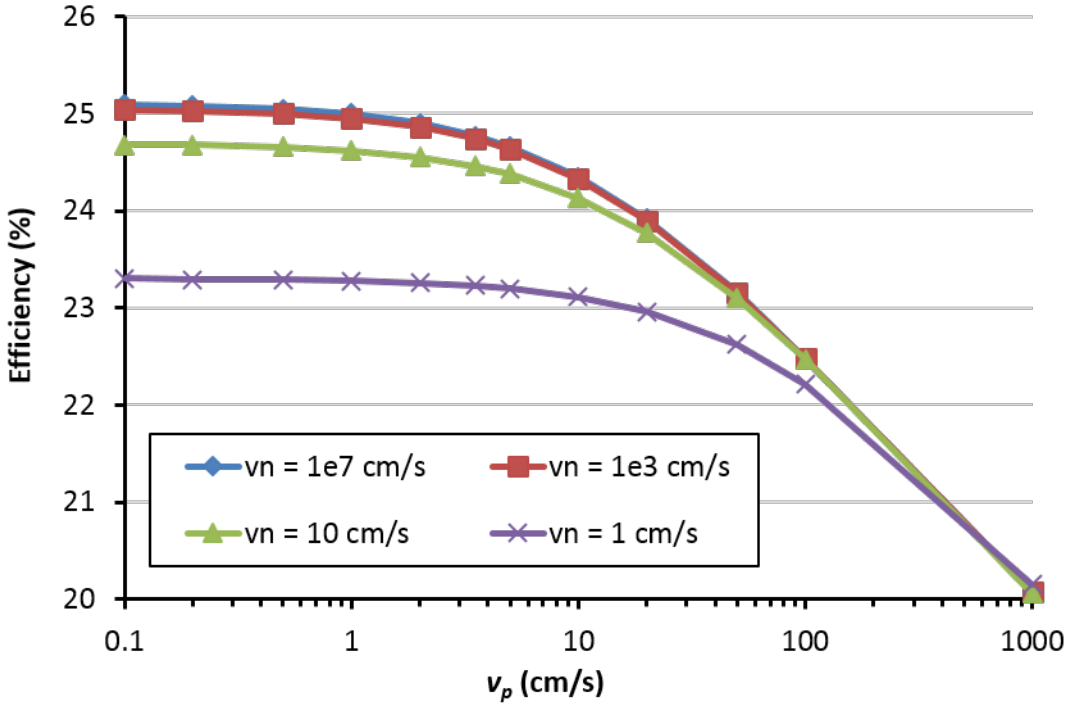



**Figure 95:** Modeled TOPCon cell efficiency as function of majority carrier (electron) velocity $v_n$ and minority carrier (hole) velocity $v_p$.

red curve in Figure 96.

Third step of the modeling involves $J'_{ob}$ measurement. Fraunhofer measured a $J'_{ob}$ value of 8±2 fA/cm$^2$ from a symmetric TOPCon test structure composed of a thin (∼1.5 nm) tunnel oxide/n$^+$ Poly-Si stack on both sides of a wafer as described in [12, 13]. The measured $J'_{ob}$ value of 8±2 fA/cm$^2$ was used to obtain a $v_p$ value of 3.5±0.8 cm/s from the red curve in Figure 96. Note that metal should have little or no effect on the $J'_{ob}$ value of the TOPCon structure because metal is physically decoupled from the base by the tunnel oxide. Therefore, we can use the measured $J'_{ob}$ value from the test structure (no metal) to extract $v_p$ for the cell modeling. Once all the parameters were established in Table 28, including $v_p$ of 3.5 cm/s, Sentaurus model was run to obtain cell IV parameters. Table 29 shows that an excellent match was obtained between the measured and calculated $V_{oc}$, $J_{sc}$, $FF$ and efficiency.

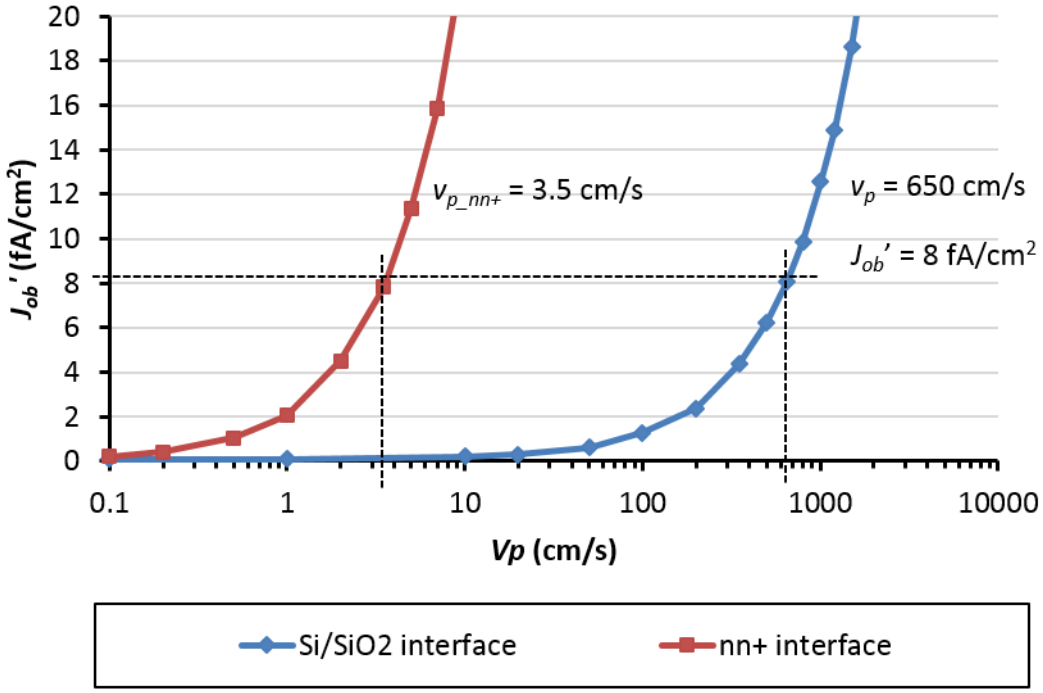



**Figure 96:** $J'_{ob}$ as function of $v_p$ at the Si/$SiO_2$ (with in-diffused phosphorus profile) and $nn^+$ interface (without in-diffused phosphorus profile.)

**Table 29:** Comparison of Measured and Modeled Photolithography Contacts Solar Cell IV Parameters

| ID | $V_{oc}$ (mV) | $J_{sc}$ (mA /cm$^2$) | $FF$ (%) | Eff. (%) | n-factor | Total $R_s$ |
|---|---|---|---|---|---|---|
| Experiment | 718 | 41.5 | 83.4 | 24.9 | [1]0.95 | [2]0.37 |
| Model | 715 | 41.5 | 83.5 | 24.8 | 0.98 | 0.30 |

[1] Calculated from Suns-$V_{oc}$ measurement using $V_{oc}$ and $J_{sc}$ at 1 sun and 0.1 sun. [2] Estimated from $FF$ and n-factor.

It has been shown in [125] that during the 850-900 °C anneal of the deposited $n^+$ Poly-Si layer, some phosphorus diffuses through the tunnel oxide. In order to assess its impact and implication, we reused the above methodology steps by incorporating the measured phosphorus diffusion profile (Figure 97: $N_s$ ~$4\times10^{18}$ cm$^{-3}$ and depth of ~0.07 $\mu$m) in the base at the oxide/Si interface. This generated second $J'_{ob}$ vs $v_p$ curve shown in blue curve in Figure 96. From this curve and the measured $J'_{ob}$ value of 8±2 fA/cm$^2$, a new $v_p$ value of 650±150 cm/s was obtained at the oxide/Si

interface. By using combination of the diffused $n^+$ profile and $v_p$ value of 650 cm/s at the $Si/SiO_2$ interface, we got identical light IV parameters as in the case of red curve without the diffusion profile and $v_p$ of 3.5 cm/s. This indicates that the $v_p$ value at the $n^+$-Si/tunnel oxide interface is actually ~650 cm/s, but the presence of the lightly diffused $n^+$ region acts like BSF to lower the $v_p$ value to 3.5 cm/s at the $n/n^+$ interface. Thus you can model the cell with or without the BSF profile by adjusting the recombination velocity properly at the $Si/SiO_2$ interface. In both cases, $v_p$ value at the $n/n^+$ interface remains 3.5 cm/s.

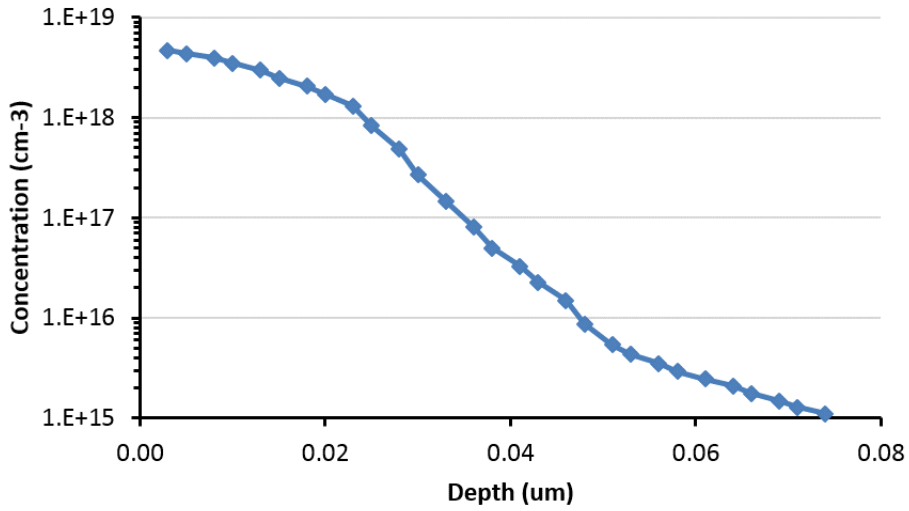



**Figure 97:** Phosphorus in-diffused profile by high temperature $n^+$ Poly-Si anneal.

## *10.2 Modeling of Screen-printed n-type PERT Cell*

In order to obtain more realistic inputs for modeling the TOPCon Cz cell, we fabricated, characterized and modeled a n-type PERT (passivated emitter, rear totally-diffused) solar cell with homogeneous 90 Ω/sq boron emitter on front and phosphorus-doped BSF on the back (Figure 98). Local metal contacts to $n^+$ BSF were formed through a $SiO_2/SiN_x$ passivating dielectric stack by laser ablation and PVD (physical vapor deposition) sputtering of Al. The PERT cell processing details can be found

in [101]. For this particular cell, front contacts were formed by screen printing with five busbars. Since back side had full area $n^+$ diffusion and local metal contacts to the absorber, the performance of this cell was significantly limited by these regions.

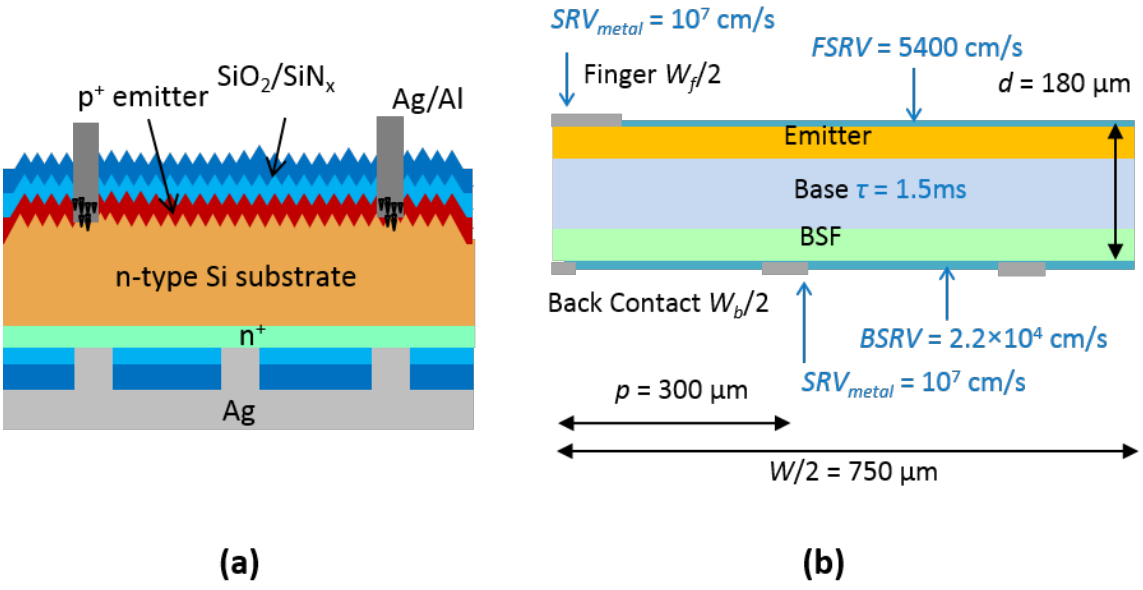



**Figure 98:** (a) Schematic diagram of a n-type solar PERT cell. (b) The cross-section of the unit cell of 21% n-type PERT solar cell used in Sentaurus 2D Modeling.

The 21% n-type PERT cell was modeled first using the Sentaurus 2D device model [29], which gave excellent match between the modeled and experimental IV data (Table 31). The unit cross-section of the n-type PERT solar cell structure used in the modeling is shown in Figure 98 (b), and all the key modeling parameters are listed in Table 30. It is important to note that the actual front finger width was 55 $\mu$m, but an effective front finger width of 98.2 $\mu$m was used in the modeling to account for the metal contribution from the five busbars with a metal coverage of ~2.8%. This resulted in total metal coverage of 6.5%. Busbar width was 0.9 mm in the real device. Using the emitter profile (Figure 99, a), $J_{oe}$ versus Front Surface Recombination Velocity ($FSRV$) curve was obtained by the Sentaurus Device model [22, 23] (Figure 99, b).

The $FSRV$ of 5400 cm/s was then extracted from the Figure 99 (b) curve and

**Table 30:** Important Input Parameters for Modeling N-type PERT Cell by Sentaurus 2D Device Model

| Sentaurus Parameters | 21% n-type PERT |
|---|---|
| Front Finger Width /Effective Front Finger Width $W_f$ ($\mu$m) | 55/98.2 |
| Front Finger Spacing $W$ (mm) | 1.5 |
| Thickness $d$ ($\mu$m) | 180 |
| Optical Reflection and Generation Profile | [1]Ray tracing |
| Back Contact Width $W_b$ ($\mu$m) | [2]3.4 |
| Back Contact Spacing $p$ ($\mu$m) | 300 |
| Emitter Profile | ECV-measured |
| Emitter Sheet Resistance ($\Omega$/sq) | $\sim$90 |
| Emitter Surface Concentration $N_s$ (cm$^{-3}$) | $2.9\times10^{19}$ |
| Emitter Junction Depth ($\mu$m) | $\sim$0.45 |
| Base Doping (cm$^{-3}$) | $9.2\times10^{14}$ |
| Base Resistivity ($\Omega$-cm) | 5 |
| BSF Profile | ECV-measured |
| BSF Sheet Resistance ($\Omega$/sq) | $\sim$75 |
| BSF Surface Concentration (cm$^{-3}$) | $7.5\times10^{19}$ |
| BSF Junction Depth ($\mu$m) | $\sim$0.45 |
| Contact Surface Recombination Velocity $SRV_{metal}$ (cm/s) | $10^7$ |
| Front Surface Recombination Velocity $FSRV$ (cm/s) | 5400 |
| Lifetime $\tau$ (ms) | 1.5 |
| Back Surface Recombination Velocity $BSRV$ (cm/s) | $2.2\times10^4$ |
| Back Specific Contact Resistance (m$\Omega$-cm$^2$) | [3]$\leq$1 |
| Series Resistance for Front Contact, Fingers and Busbars $R'_s$ ($\Omega$-cm$^2$) | 0.13 |

[1]We were using Phong reflection model for internal reflection with Rphong and wphong as 0.98 and 200, respectively [35]. [2]3.4 $\mu$m width 300 $\mu$m spacing line contact has almost the same metal coverage as experimental 32 $\mu$m diameter 300 $\mu$m spacing point contact. [3]Specific contact resistance is extracted by comparing measured series resistance from different back spacing cells.

**Table 31:** Comparison of Measured and Modeled Screen-printed N-type PERT Solar Cell IV Parameters

| ID | $V_{oc}$ (mV) | $J_{sc}$ (mA /cm$^2$) | $FF$ (%) | Eff. (%) | n-factor | Total $R_s$ |
|---|---|---|---|---|---|---|
| Experiment | 658.8 | 39.2 | 81.2 | 21.0 | 1.05 | 0.42 |
| Model | 658.5 | 39.2 | 81.3 | 21.0 | 1.06 | 0.39 |

the measured $J_{oe}$ of $\sim$80 fA/cm$^2$ on a symmetric test structure with identical emitter and passivation on both sides. This methodology is described in detail in [21, 26]. A

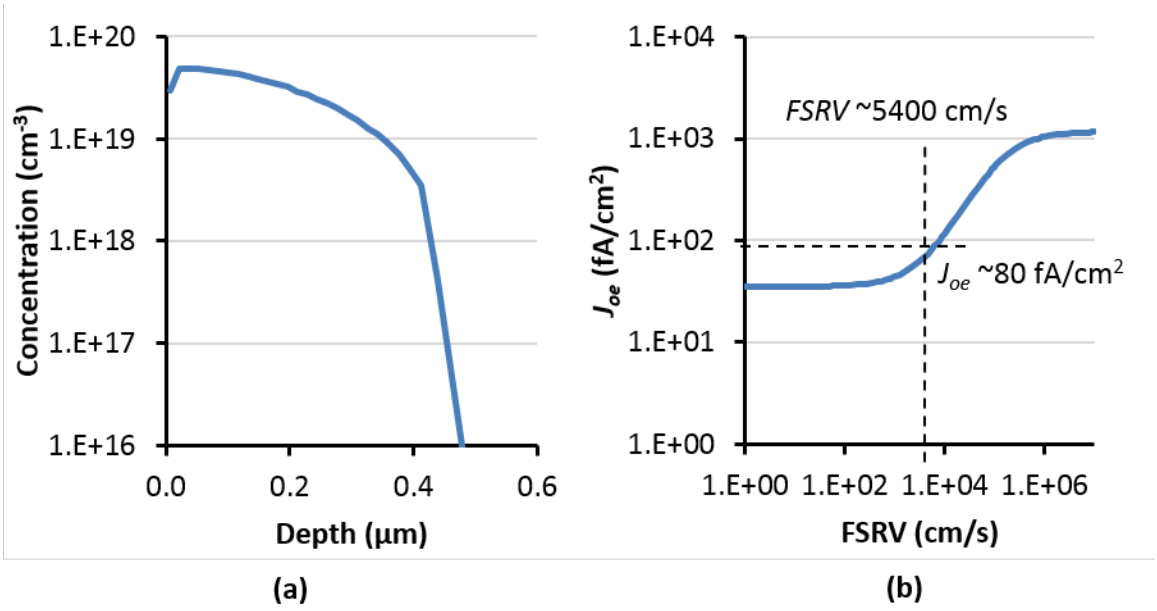



**Figure 99:** (a) Emitter profiles for the 90 Ω/sq emitter. (b)The model $J_{oe}$ vs $FSRV$ curves for the 90 Ω/sq emitter.

lifetime of 1.5 ms was estimated from the finished effective lifetime measurement (tau intercept) on a test structure that went through exactly the same high temperature processing. An effective Back Surface Recombination Velocity ($BSRV$) of $2.2\times10^4$ cm/s was extracted by matching the measured $V_{oc}$ after $FSRV$ and lifetime were fixed. Series resistance contribution from front contact, fingers and busbars ($R'_s$) was extracted by using test structures and the methodology described in [21, 88, 8]. Note that $R'_s$ does not include the sheet, bulk, and back contact resistance. The $J_{oe}$ and $J_{ob}$ were extracted to be ∼150 and ∼140 fA/cm$^2$, respectively, for the fabricated 21% efficient n-type PERT cell (Section 10.3.2).

## *10.3 Modeling of Manufacturable Screen-printed n-type TOPCon Cell*

### 10.3.1 Passivated Back Contact

After achieving the excellent match between the measured and modeled parameters of the 24.9% photolithography TOPCon cell (Table 28) and the 21.0% screen-printed

**Table 32:** Important Input/Output Parameters for Sentaurus 2D Device Model of Manufacturable Screen-printed N-type TOPCon Cell

| Sentaurus Parameters | Homogeneous Emitter TOPCon | Selective Emitter TOPCon | Thin Finger and Better Material |
|---|---|---|---|
| $V_{oc}$ (mV) | 671.3 | 706.5 | 709.7 |
| $J_{sc}$ (mA/cm$^2$) | 39.3 | 39.3 | 39.7 |
| $FF$ (%) | 81.8 | 81.2 | 82.3 |
| Efficiency (%) | 21.6 | 22.6 | 23.2 |
| n-factor | 1.08 | 1.15 | 1.03 |
| Total $R_s$ ($\Omega$-cm$^2$) | 0.28 | 0.41 | 0.44 |
| Effective Front Finger Width $W_f$ ($\mu$m) | 98.2 | 55 | 40 |
| Front Shading Width ($\mu$m) | 98.2 (6.5%) | 98.2 (6.5%) | 83.2 (5.5%) |
| Front Finger Spacing $W$ (mm) | 1.5 | 1.5 | 1.5 |
| Thickness ($\mu$m) | 180 | 180 | 180 |
| Field Emitter Profile | Measured | Measured | Measured |
| Field Emitter Sheet Resistance ($\Omega$/sq) | $\sim$90 | $\sim$150 | $\sim$150 |
| Field Emitter Surface Concentration (cm$^{-3}$) | $2.9\times10^{19}$ | $4.8\times10^{18}$ | $4.8\times10^{18}$ |
| Field Emitter Junction Depth ($\mu$m) | $\sim$0.45 | $\sim$1.65 | $\sim$1.65 |
| Selective Emitter Profile | N/A | Measured | Measured |
| Selective Emitter Sheet Resistance ($\Omega$/sq) | N/A | $\sim$20 | $\sim$20 |
| Selective Emitter Surface Concentration (cm$^{-3}$) | N/A | $\sim3\times10^{19}$ | $\sim3\times10^{19}$ |
| Selective Emitter Junction Depth ($\mu$m) | N/A | $\sim$3 | $\sim$3 |
| Selective Emitter Junction Width $W_{SE}$ ($\mu$m) | N/A | 100 | 100 |
| Substrate Doping (cm$^{-3}$) | $9.2\times10^{14}$ | $9.2\times10^{14}$ | $4.5\times10^{14}$ |
| Substrate Resistivity ($\Omega$-cm) | 5 | 5 | 10 |
| Field FSRV $FSRV_{field}$ (cm/s) | 5400 | 350 | 350 |
| Wing FSRV $FSRV_{wing}$ (cm/s) | N/A | 700 | 700 |
| Front Contact FSRV $SRV_{metal}$ (cm/s) | $10^7$ | $10^7$ | $10^7$ |
| Lifetime $\tau$ (ms) | 1.5 | 1.5 | 3 |
| Back Specific Contact Resistance (m$\Omega$-cm$^2$) | 5 | 5 | 5 |
| Series Resistance for Front Contact, Fingers and Busbars ($\Omega$-cm$^2$) | 0.13 | 0.13 | 0.15 |
| Measured $J'_{ob}$ (fA/cm$^2$) | 8 | 8 | 8 |
| Back Contact Electron SRV $BSRV.v_n$ (cm/s) | $10^7$ | $10^7$ | $10^7$ |
| In-Diffused Back Surface Field Profile | Measured | Measured | Measured |
| Back Contact Hole SRV at n$^+$ Si/ tunnel oxide interface $BSRV.v_{p-n^+ox}$ (cm/s) (cm/s) | 650 | 650 | 650 |

PERT cell (Table 30), we combined the two models to estimate the efficiency potential of manufacturable screen-printed TOPCon cell on commercial grade Cz material. To do so, we replaced the emitter and contact parameters of the 24.9% TOPCon cell in the model with our current manufacturable screen-printed 21% cell parameters in addition to Fz material properties replaced by commercial grade Cz Si. Back side TOPCon properties were kept the same. The unit cell cross-section of this manufacturable screen-printed Cz TOPCon solar cell (homogeneous boron emitter, n-type Cz base, and TOPCon on the back) is shown in Figure 100. All the realistic input parameters and the model outputs are shown in Table 32, column 2 called "Homogeneous Emitter TOPCon".

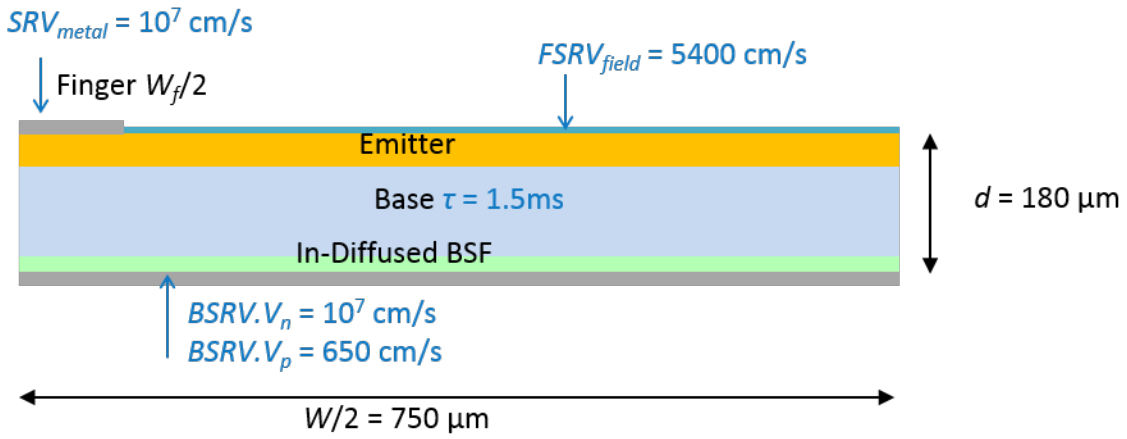



**Figure 100:** The cross-section schematic scheme of the 21.6% n-type screen-printed TOPCon solar cell for Sentaurus 2D Modeling.

Notice that all the input parameters for the base, emitter and screen-printed front contact regions are measured or extracted from the fabricated 21.0% n-type screen-printed PERT cell in Section 10.2 and summarized in Table 30. Modeling results show that the cell efficiency increased from this 21.0% PERT cell to only 21.6% with $V_{oc}$ from 659 to 671 mV, $J_{sc}$ from 39.2 to 39.3 mA/cm$^2$ and $FF$ from 81.3 to 81.8%, by replacing the the full area BSF and local contacts (to the p$^+$ back) by the TOPCon structure ($J'_{ob}$= 8 fA/cm$^2$ and $v_p$= 650 cm/s with n$^+$ diffusion obtained from the

24.9% cell modeling) in the model. $FF$ increased by 0.5% compared to the PERT cell because the series resistance ($R_s$) decreased by 0.1 Ω-cm$^2$, from 0.39 to 0.28 Ω-cm$^2$, due to one dimensional current flow at the full area back contact. In the case of PERT cell, carriers have to flow laterally on the back to get to local contacts. $V_{oc}$ increased by 12 mV because the total $J_o$ decreased from ~290 to only ~173 fA/cm$^2$, because $J'_{ob}$ decreased from 125 to 8 fA/cm$^2$ (as latter summarized in Figure 107). However, the $J_{oe}$ value remained very high (150 fA/cm$^2$). This shows that the device performance of this screen-printed Cz TOPCon cell is limited by the homogeneous emitter. Therefore, the next step in the modeling involved implementing selective emitter to realize the full potential of passivated contact in diffused front junction screen-printed cell with TOPCon back.

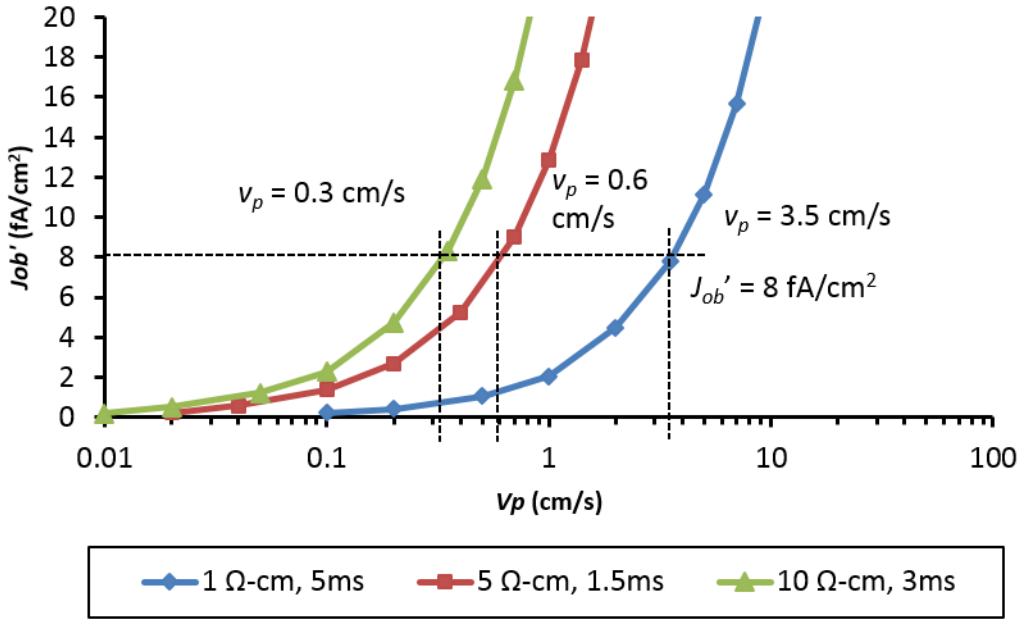



**Figure 101:** $J'_{ob}$ as function of $v_p$ for different materials (resistivity and lifetime) without the in-diffused phosphorous BSF profile.

Next we generated $J'_{ob}$ vs $v_p$ curves for different resistivity and lifetime materials in Figure 101 using the methodology described earlier. Notice that $v_p$ changes with the base material properties for the same TOPCon properties. For example, a $v_p$

of 0.6 cm/s was extracted at $n/n^+$ interface for 5 Ω-cm Cz material for the same 8 $fA/cm^2$ $J'_{ob}$ compared to 3.5 cm/s for 1 Ω-cm Fz material. This can be explained by $J_{ob} = \frac{qn_i^2}{N_D}v_p$, where $v_p$ at $n/n^+$ interface needs to be changed with $N_D$ for the same $J'_{ob}$. In modeling with BSF, this is automatically calculated by Sentaurus since 5 Ω-cm TOPCon cell has larger $nn^+$ step compared to 1 Ω-cm doping (for the same BSF profile) which gives lower $v_p$ at $n/n^+$ interface (Figure 102). Even though $v_p$ changes, $J'_{ob}$ value for a given TOPCon structure has been found to be independent of base material properties in our lab [126, 127, 128]. Also note that the same carrier generation profile was used for the 21% n-type PERT cell and the TOPCon cell because the measured escape reflectance is similar (Figure 103) for both the cells [127].

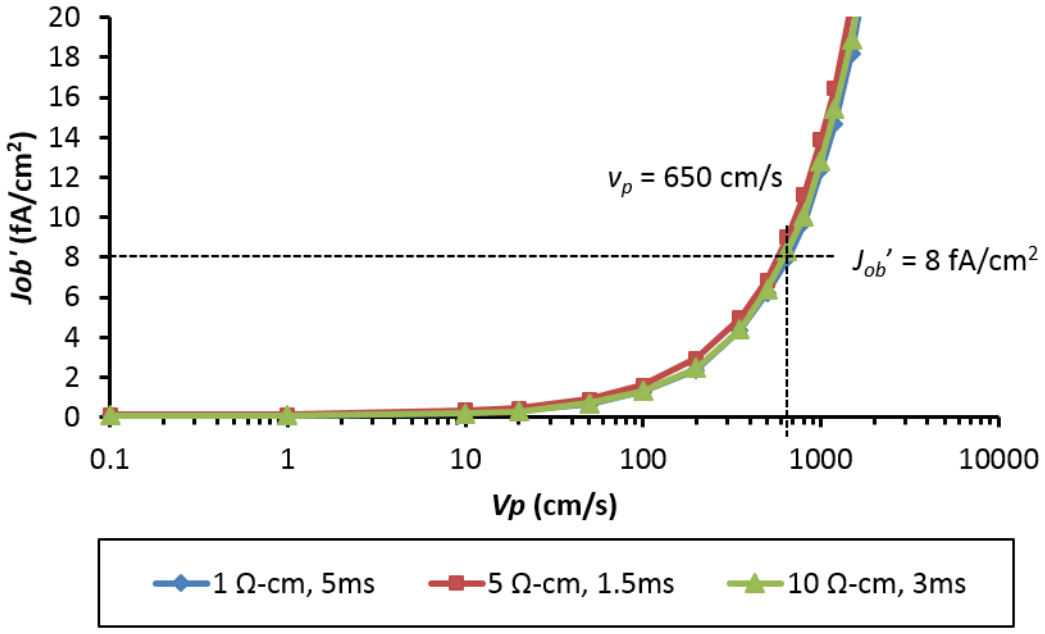



**Figure 102:** $J'_{ob}$ as function of $v_p$ for different materials (resistivity and lifetime) with the in-diffused phosphorous BSF profile.

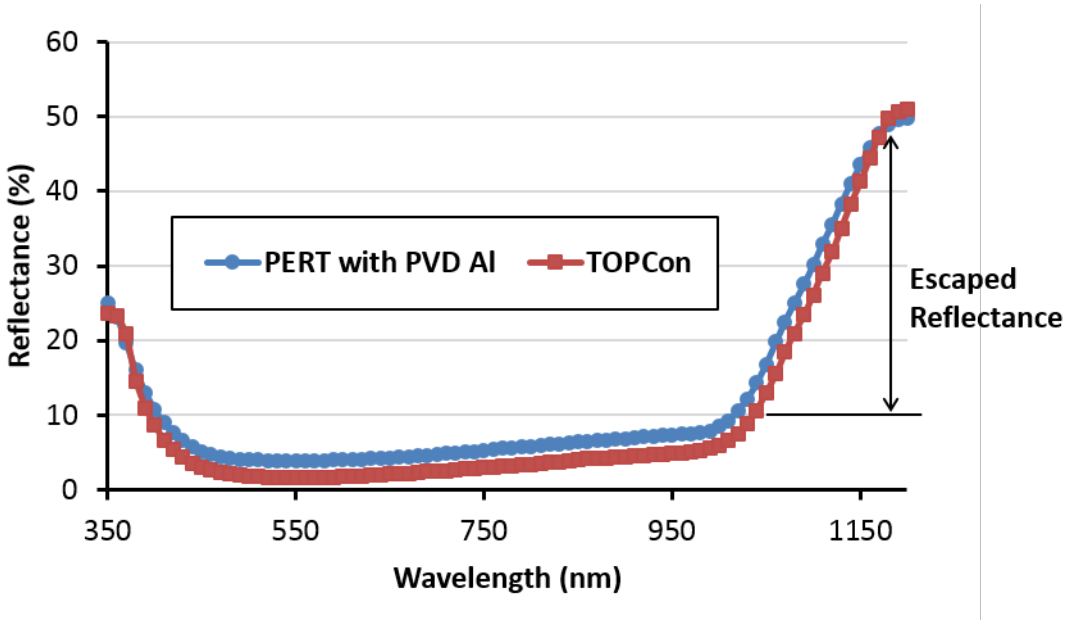



**Figure 103:** The measured total/escaped reflectance of PERT and TOPCon n-type solar cells.

### 10.3.2 Understanding and Modeling the Impact of Incorporating Boron Selective Emitter on Screen-printed TOPCon Cell

Since the performance of 21.6% TOPCon cell with homogeneous boron emitter was limited by $J_{oe}$. In this section, selective emitter design was incorporated into the 2D Sentaurus model to reduce $J_{oe}$ and quantify its impact on efficiency enhancement of screen-printed TOPCon Cz cell. Selective emitter profiles and $FSRV$ parameters were taken from the 24.9% cell modeling in Table 28. The schematic cross-section of the unit cell of the selective emitter TOPCon solar cell structure is shown in Figure 104.

However, the selective emitter width ($n^{++}$ width) was increased from 12 to 100 $\mu$m for a more realistic industrial process. Metal finger width was also changed from $\sim$16 to $\sim$55 $\mu$m along with the increase in finger spacing from 0.8 to 1.5 mm to stay consistent with our current manufacturable screen-printing contact technology. All the remaining modeling parameters were unchanged and are summarized in Table 32, column 3 called "Selective Emitter TOPCon". Note that Sentaurus model predicted

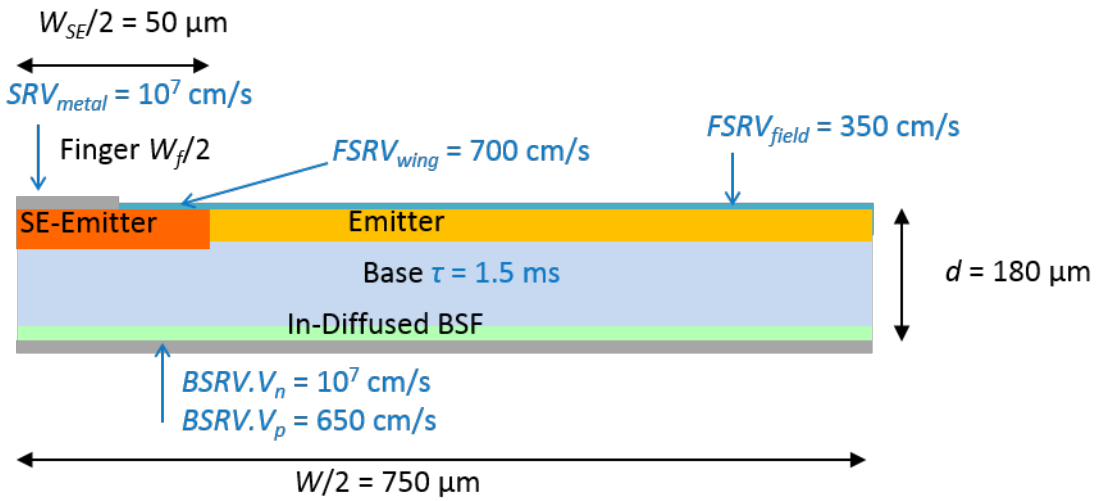
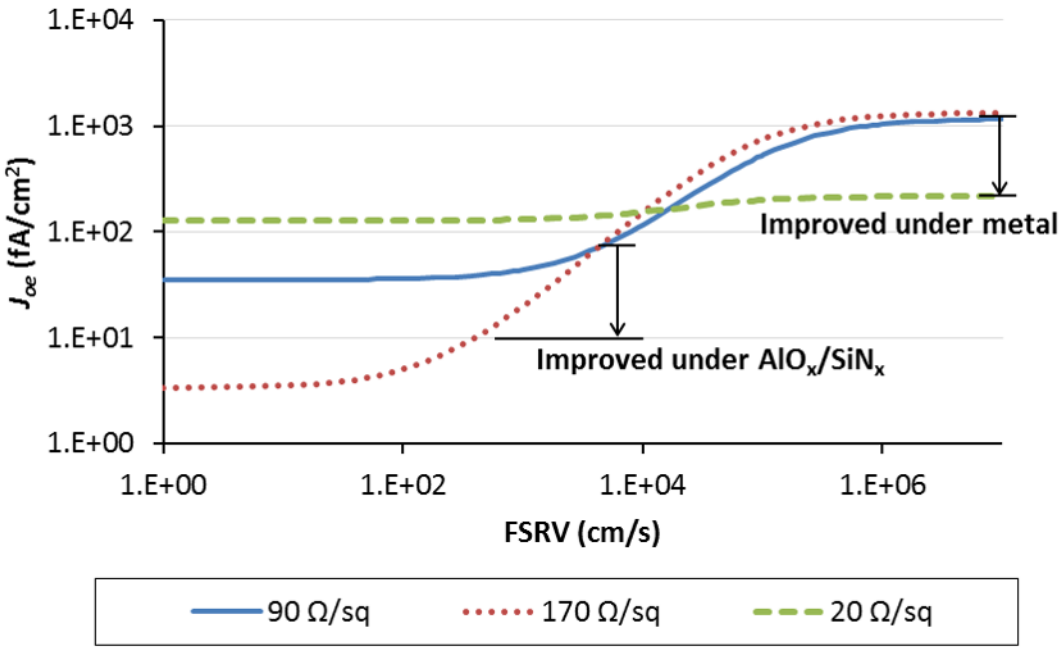



**Figure 104:** The cross-section schematic scheme of the 22.6% screen-printed TOPCon solar cell for Sentaurus 2D Modeling.

an efficiency of 22.6% for this cell with $V_{oc}$ of 707 mV, $J_{sc}$ of 39.3 mA/cm$^2$, and $FF$ of 81.2%. It is important to recognize that selective emitter provides 1% absolute efficiency enhancement over the homogeneous emitter TOPCon cell whose performance was limited by the emitter $J_{oe}$. Model calculations show an increase of ∼36 mV in $V_{oc}$ due to selective emitter incorporation which decreases total $J_o$ from ∼173 to ∼45 fA/cm$^2$ and $J_{oe}$ from ∼150 to ∼22 fA/cm$^2$.

In order to quantify and understand the significant drop in $J_{oe}$, we analyzed the $J_{oe}$ contribution from different regions of the selective and homogeneous emitter. Figure 105 shows the modeled $J_{oe}$ vs $FSRV$ curves for the 90 Ω/sq homogeneous emitter, and 150 Ω/sq and 20 Ω/sq regions of the selective emitter. These are calculated [23, 22] from the Sentaurus model using the measured profiles as shown in Figure 106. Since underneath the metal $FSRV$ is ∼$10^7$ cm/s, these curves give $J_{oe}$ of 1160 fA/cm$^2$ for the 90 Ω/sq profiles. Using the 6.5% metal coverage for the PERT cell, we obtain a metal contribution of 75 fA/cm$^2$ to the $J_{oe}$ of homogeneous emitter. This combined with the measured unmetallized $J_{oe}$ of 80 fA/cm$^2$ for the 90 Ω/sq emitter with 93.5% field area, field contribution to $J_{oe}$ is calculated to be 75 fA/cm$^2$.




| Region | Emitter Rsheet (Ω/sq) | Emitter Profile | Passivation | *FSRV* (cm/s) | $J_{oe}$ (fA/cm²) | Area (%) | Contribution to $J_{oe}$ (fA/cm²) | Total $J_{oe}$ (fA/cm²) |
|---|---|---|---|---|---|---|---|---|
| Field | 90 | Measured | $SiO_2/SiN_x$ | 5400 | 80 (measured) | 93.5 | 75 | 150 |
| Metal | 90 | Measured | Metal | $10^7$ | 1160 | 6.5 | 75 | |
| Field | 170 | [1]Model | $AlO_x/SiN_x$ | 400 | 10 (measured) | 93.3 | 9 | |
| Wing | 20 | FhG ISE | $AlO_x/SiN_x$ | [2]700 | 130 | 3 | 4 | 21 |
| Metal | 20 | FhG ISE | Metal | $10^7$ | 220 | 3.7 | 8 | |

[1] The 170 Ω/sq emitter profile was obtained by Sentaurus Process with the experimental ion implanted dose and energy, and the annealing conditions as inputs. [2] 700 cm/s is estimated from Hoex's $AlO_x$ passivation data on $2.6\times10^{19}$ $cm^{-3}$ surface concentration with textured surface.

**Figure 105:** The model $J_{oe}$ vs FSRV curves for the 90 Ω/sq, 150 Ω/sq and 20 Ω/sq emitters.

This results in total $J_{oe}$ of 150 fA/cm$^2$ for the modeled 21.6% homogeneous emitter TOPCon cell. In the case of selective emitter device, $J_{oe}$ metal is reduced to 217 fA/cm$^2$ at $FSRV$ of $\sim 10^7$ cm/s (Figure 105) because of the 20 Ω/sq emitter. The metal/Si contact area is only 2.8% due to metal fingers alone because floating busbars do not contact Si but reside on the dielectric. Therefore, the metal contribution to $J_{oe}$ is only about 8 fA/cm$^2$ in selective emitter cell. From the Hoexs data of $Al_2O_3$ passivated boron emitters [24], a 20 Ω/sq $n^{++}$ diffusion with surface concentration ($N_s$) of $\sim 3 \times 10^{19}$ cm$^{-3}$ should have an $FSRV$ ~700 cm/s. This gives a $J_{oe}$ of 128

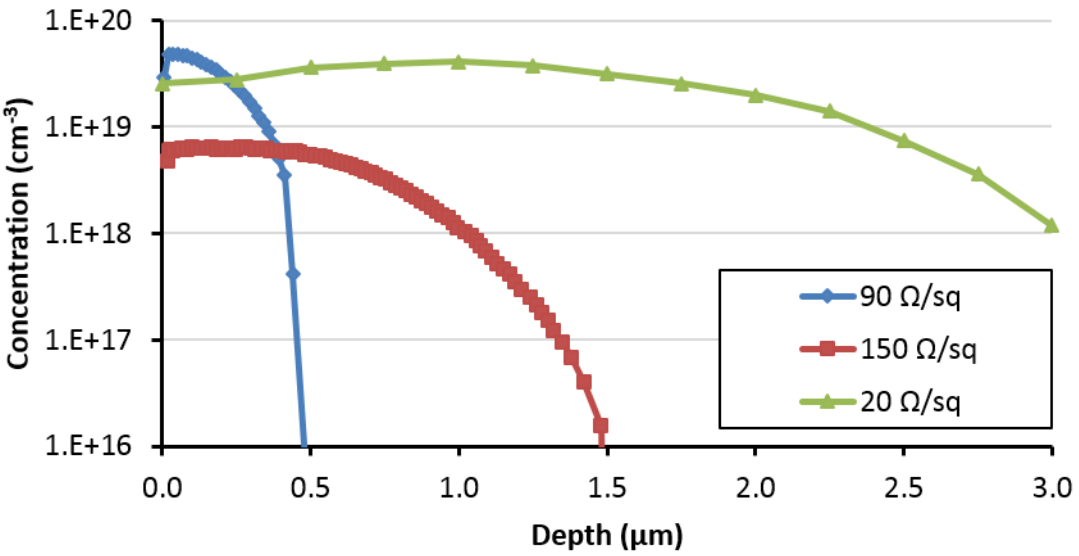



**Figure 106:** Emitter profiles for the 90 Ω/sq, 150 Ω/sq and 20 Ω/sq emitters.

fA/cm$^2$ from Figure 105. Since the unmetallized portion of the 100 $\mu$m n$^{++}$ selective diffused region accounts for only 3% of the area coverage, its contribution to $J_{oe}$ is 4 fA/cm$^2$. $J_{oe}$ of the unmetallized 150 Ω/sq n$^+$ field region was measured to be 12±2 fA/cm$^2$ by making symmetrically diffused and passivated samples and testing them by QSSPC technique using the Sinton tool [114]. Figure 105 shows that this corresponds to a $FSRV$ of ∼350 cm/s. Since field region accounts for 93.3% area (20 Ω/sq 100 $\mu$m wide n$^{++}$ diffused region accounts for remaining 6.7%), its contribution to $J_{oe}$ is 10 fA/cm$^2$. This gives a total $J_{oe}$= 8+4+10= 22 fA/cm$^2$ compared to 150 fA/cm$^2$ for the 90 Ω/sq homogeneous emitter cell. Figure 105 also summarizes the above analysis with various $J_{oe}$ components. This analysis shows that the modeled 22.6% selective emitter TOPCon cell on Cz has a total $J_o$= 45 fA/cm$^2$ with $J_{oe}$= 22 fA/cm$^2$ and $J_{ob}$= 23 fA/cm$^2$ compared to the 21.6% homogeneous emitter TOPCon cell, which has total $J_o$= 173 fA/cm$^2$ with $J_{oe}$= 150 fA/cm$^2$ and $J_{ob}$= 23 fA/cm$^2$.

Table 33 summarizes the main difference between the key material and device parameters of a 22.6% manufacturable screen-printed TOPCon cell and the 24.9% laboratory cell with photolithography contacts. These parameters include front contact

metal shading, finger spacing, selective emitter width, cell thickness, base resistivity, bulk material lifetime, and the resulting n-factor and total $R_s$.

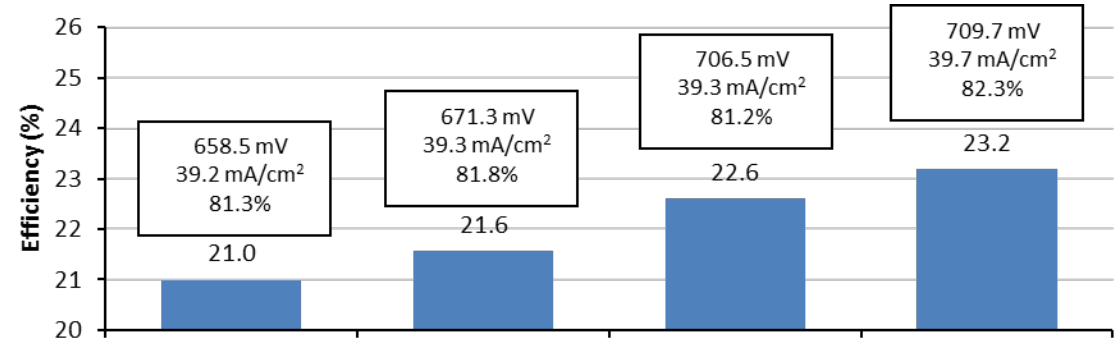
**Table 33:** Comparison of Photolithography and Screen-Printed Contact TOPCon Cell

| Parameter | PL TOPCon | Screen-printed TOPCon |
|---|---|---|
| $V_{oc}$ (mV) | 715 | 706.5 |
| $J_{sc}$ (mA/cm$^2$) | 41.5 | 39.3 |
| $FF$ (%) | 83.5 | 81.2 |
| Efficiency (%) | 24.8 | 22.6 |
| Front Metal Shading (%) | 2.5 | 6.5 |
| Finger Spacing (mm) | 0.8 | 1.5 |
| Finger Width ($\mu$m) | 16 | 55 |
| Selective Emitter Width ($\mu$m) | 12 | 100 |
| Thickness ($\mu$m) | 200 | 180 |
| Resistivity ($\Omega$-cm) | 1 | 5 |
| Lifetime (ms) | 5 | 1.5 |
| n-factor | 0.98 | 1.15 |
| total $R_s$ ($\Omega$-cm$^2$) | 0.30 | 0.41 |

### 10.3.3 Exploring the Limit of Above Front Junction Single Side TOPCon Cell on Commercial Grade Cz Si with Screen-printed Contacts and Boron Selective Emitter

In order to understand the efficiency limit of the above single side TOPCon Cz cell structure, we incorporated three realistic improvements in our model that can happen in the near future. We changed the screen-printed line width from 55 to 40 $\mu$m [129], improved the base material quality to 10 $\Omega$-cm resistivity with 3 ms bulk lifetime. In addition, we increased $R'_s$ from 0.13 to 0.15 $\Omega$-cm$^2$ to account for the thinner fingers. All the input parameters for the modeled 23.2% cell are listed in Table 32, column 4 referred to as "Thin Finger and Better Material". With these changes, our model predicted an efficiency of 23.2% with Voc of 710 mV, Jsc of 39.7 mA/cm2, and FF of 82.3%. The extracted $J_{oe}$ and $J_{ob}$ values were 22 and 18 fA/cm$^2$ for this device, respectively. Figure 107 shows a technology roadmap to drive the efficiency of a 21%

traditional n-PERT cell with homogeneous emitter to 23.2% single side TOPCon cell with selective emitter.




| | nPERT | 90 Ω/sq TOPCon (Homo. Emitter) | Selective Emitter (150 & 20 Ω/sq) | Thin Finger & Better Material |
|---|---|---|---|---|
| *Joe.metal | 75 | 75 | **10** | 10 |
| *Joe.pass | 75 | 75 | **8** | 8 |
| *Joe.wing | n/a | n/a | **4** | 4 |
| *Job.bulk | 15 | 15 | 15 | **10** |
| *Job' | 125 | **8** | 8 | 8 |
| *Jo.total | **290** | **173** | **45** | **40** |
| | 55 µm 1.5 mm spacing<br>non-foating bus<br>6.5% metal &shading<br>~90 Ω/sq emitter<br>5 Ω-cm, 1.5ms<br>*FSRV* ~5400cm/s<br>Job' ~ 125 fA/cm² | Job' ~ 8 fA/cm²<br>In-Diffused BSF<br>*BSRV.V$_n$* ~1e7 cm/s<br>*BSRV.V$_p$* ~650 cm/s | floating bus<br>3.7% metal<br>6.5% shading<br>150 & 20 Ω/sq emitter<br>100 µm wing width<br>*FSRV.field* ~350 cm/s<br>*FSRV.wing* ~700 cm/s | 40 µm 1.5 mm spacing<br>2.7% metal<br>5.5% shading<br>10 Ω-cm, 3 ms<br><br>*All the *Jo* values are in the unit of fA/cm² |

**Figure 107:** The calculated efficiency improvements from 21% n-type PERT to 23.2% TOPCon solar cell. All the important model inputs and outputs parameters are also listed for comparison.

## *10.4 Summary*

In this task, a methodology for modeling the next generation tunnel oxide passivated TOPCon cell was established using the Santaurus 2D model, which involves replacing the TOPCon region by carrier selective electron and hole recombination velocities to match the measured $J'_{ob}$ of the TOPCon region as well as all the light IV parameters ($J_{sc}$, $V_{oc}$, $FF$, and efficiency) of the TOPCon cell. This approach was validated by modeling a 24.9% small area TOPCon cell with photolithography contacts on Fz Si

fabricated by Fraunhofer ISE. TOPCon modeling was extended to large area commercial grade Cz material with screen-printed contacts using the actual material and device parameters from the 21% bench mark n-type cell fabricated and modeled in our lab. It was found that the cell efficiency increases to only 21.6% if we apply the TOPCon structure on the back of this 21% n-PERT with conventional 90 Ω/sq homogeneous emitter with screen-printed contacts on the front. This is because efficiency of this device was limited by the emitter $J_{oe}$ of ∼150 fA/cm$^2$ with total $J_o$ of ∼173 fA/cm$^2$. However, if a selective emitter is applied on the front to lower the $J_{oe}$ from ∼150 to ∼22 fA/cm$^2$ (by using a combination of 150 and 20 Ω/sq emitters with $AlO_x$/$SiN_x$ passivation), cell efficiency of 22.6% can be achieved with TOPCon back on a commercial Cz material. Finally, modeling shows that 23.2% efficiency can be achieved with this rear side TOPCon cell structure on Cz if screen-printed finger width can be reduced from 55 to 40 $\mu$m, and 10 Ω-cm 3 ms lifetime base material is used.

# CHAPTER XI

# CONCLUSION AND FUTURE WORK

This thesis covered some of the most exciting and active areas of research in Si PV for achieving low-cost high-efficiency Si solar cell. Since Si material accounts for 30-33% of the module cost, we studied three specific strategies to lower the Si material cost in a finished module without sacrificing efficiency.

First approach involves development of high efficiency low-medium concentrator Si solar cells to reduce the required Si material for the same output power. In Task 1, we have developed a methodology and applied it to generate Highest Achievable Efficiency (HAE) curve at 1-20X concentration in order to optimize the front metal pattern design of screen-printed concentrator Si solar cells. The model was validated by fabricating some concentrator Si solar cells. At the start of Task 1, a commercial baseline screen-printed technology was used to produce 18.3% efficient cells at one sun. It was demonstrated that this efficiency can be increased to 19.0% at 4-5X with 1.63 mm finger spacing for 25 mm effective finger length. In addition, an efficiency of 18.0% at 20X was also demonstrated. It was found that efficiency of these cells was limited by the 110 $\mu$m wide screen-printed fingers. Therefore, a new extrusion printing technology was implemented to print 50 $\mu$m wide Ag lines. This produced 19.0% cells at one sun and 20.2% efficient cell at $\sim$9X with 25 mm long effective fingers and spacing of 0.72 mm. This was in excellent agreement with the model calculations of the HAE at a given concentration for this technology. This represents one of the highest efficiency direct metal printed low-medium concentrator cells at the time. Finally, a roadmap to achieve $\geq$21% 3-5X efficient concentrator Si solar cell was developed for a 20.2% one-sun PERC cell structure using direct printed lines.

The second strategy in this research involves producing high efficiency cells on lower cost epi-Si wafers to eliminate the need for making expensive feedstock Poly-Si, ingot growth and wafer dicing. In Task 2, the study and optimization of PSI back reflector for thin epi-Si cells using epitaxial wafer equivalent (EpiWE) structure are shown. The refractive index and thickness requirements for a good PSI back reflector were established. Using the guideline, PSI layer was formed by controlling anodized current. Scattering factor at the epi-Si PSI interface was measured to be ∼99% in the long wavelength exceeding 1150 nm. Large area, screen-printed EpiWE cells with PSI back reflector were fabricated with 17.3% of efficiency. PC1D model is used to obtain a good match between the calculated and measured LIV, EQE and Reflectance data which gives $BSRV$ and $R_b$ values of 90 cm/s and 88%, respectively. These values are superior to the standard industrial full Al-BSF Si solar cells even though the cell fabrication processes was essentially the same. The PC1D model also showed very little drop in cell efficiency for thinner active epi-Si because of the good PSI back reflector. Model shows that efficiencies of ∼16.7% and ∼15.7% could be achieved if the cell thickness is reduced to 30 and 10 $\mu$m, respectively. These results show the compatibility of PSI in Si cell processing and the promise of EpiWE Si solar cells.

Since Si substrate was part of the EpiWE cell structure, to further reduce the cost of epi-Si solr cell, a porous Si layer transfer epi-Si technology from wafer to module is studied in Task 3. Thin wafers were prepared at Crystal Solar Inc. on a reusable substrate with porous Si layer using epitaxially grown Si. Front side of the cells was processed using standard $POCl_3$ diffusion emitter, PECVD AR coating, screen-printed contacts, and laminated with standard EVA/glass. After exfoliation of the epi-Si layer from the substrate using the PSI layer transfer process, rear side of the cell was finished by dielectric/metal deposition and laser fired contacts. A sealed edge wafer structure and texturing optimization was studied and developed to improve the over all process yield. Low temperature laser fired contact process was developed

and optimized to make the local back contact to the $p^+$ BSF. A 17.2% efficiency was achieved with the EVA/glass encapsulation, which corresponds to ∼18.0% cell efficiency without encapsulation. $BSRV$ and $R_b$ values of 150 cm/s and 87% were extracted by PC1D device modeling. Several 40-90 $\mu$m thick epi-Si semi-module cells were fabricated with 15.6-17.2% efficiency with EVA/glass encapsulation. This is the first demonstration of large area thin epi-Si cell fabrication using layer transfer technology in combination with industrial screen-printed technology.

Although some good cells were achieved in Task 3, the module assembly for the thin epi-Si solar cells were too different from the traditional Si cell and module technology. Therefore, in Task 4, high efficiency (∼20%) screen-printed Si solar cells were fabricated on both p-type and n-type epi-Si Kerfless wafers with thickness of 120-180 $\mu$m. These epi-Si wafers can save up to 50% of wafer cost compared to traditional Cz wafers. Different resistivity (2-10 Ω-cm) p-type and n-type epi-Si wafers were tested. Best p-type PERC cell efficiency of 19.7% was achieved on ∼180 $\mu$m epi-Si wafers with resistivity of ∼3.7 Ω-cm while the counter part commercial Cz cell gave 20.1% efficiency. In the case of n-type PERT cell, best efficiency of 19.8% was achieved on ∼120 $\mu$m epi-Si wafers with resistivity of ∼2.9 Ω-cm while the counter part Cz cell gave 20.0% efficiency on 160 $\mu$m thick Si. Finished bulk lifetime was analyzed by IQE measurement and device modeling. Some epi-Si materials gave bulk lifetime close to Cz; however, in most cases bulk lifetime was somewhat lower than the Cz material. The gap between the epi-Si and Cz cells can be explained primarily on the basis of resistivity and bulk lifetime. Finally, model calculations showed that the cell efficiency can be improved appreciably by improving the bulk lifetime or obtaining the right combination of lifetime and resisitivity for the process technology used in this study.

Finally in the second strategy of this research, the potential of epi-Si material and epi-grown structures for high efficiency cell is studied in Task 5. Since the doping can

be precisely controlled by the dopant gas, the various doping regions in a solar cell can be grown all at once during epi-Si deposition. In this task we first studied the epi-grown built-in BSF in a epi-Si wafer. Sentaurus 2D model was used to study the cell performance as a function of different BSF profiles in p-PERT solar cells. The model showed that the BSF needs to be carefully chosen in order to realize the full efficiency advantage over the counterpart PERC cells. With identical front, p-type PERT solar cell with a lightly doped thick boron BSF (15-30 $\mu$m, $10^{17}$-$10^{18}$ cm$^{-3}$) can give efficiency enhancement of $\sim$0.5% over the PERC cell because of higher $FF$. Following the model prediction, p-type PERT cells were fabricated on epi-grown pp$^{+}$ substrates with in-situ lightly doped thick BSF. Using identical process, PERC cells were also fabricated on p-type epi-Si and Cz wafers for comparison. Greater than 20% cells were achieved for all these devices with epi-Si PERT cell giving the highest efficiency of 20.3%. This was 0.2-0.3% higher than the PERC cells on epi-Si and Cz wafers. Finally, the impact of epi-grown emitter was studied using a three layer (emitter, base and BSF) epi-grown PERT solar cell. Modeling showed >22.7% efficiency is achievable by obtaining the right combination of base lifetime and resistivity using more advanced screen-printed technology (40 $\mu$m wide finger and 1.5% narrow busbar shading).

The third area in this thesis involves design and modeling the potential of next generation very high efficiency cells using carrier selective passivated contacts which can eliminate metal and doping induced recombination. In Task 6, a methodology for modeling the tunnel oxide passivated TOPCon cell was established using the Santaurus 2D model, which involves replacing the TOPCon region by carrier selective electron and hole recombination velocities to match the measured $J'_{ob}$ of the TOPCon region as well as all the light IV parameters ($J_{sc}$, $V_{oc}$, $FF$, and efficiency) of the TOPCon cell. This approach was validated by modeling a 24.9% small area TOPCon cell

with photolithography contacts on Fz Si fabricated by Fraunhofer ISE. TOPCon modeling was extended to large area commercial grade Cz material with screen-printed contacts using the actual material and device parameters from the 21% bench mark n-type cell fabricated and modeled in our lab. It was found that the cell efficiency increases to only 21.6% if we apply the TOPCon structure on the back of this 21% n-PERT with conventional 90 Ω/sq homogeneous emitter with screen-printed contacts on the front. This is because efficiency of this device was limited by the emitter $J_{oe}$ of ∼150 fA/cm$^2$ with total $J_o$ of ∼173 fA/cm$^2$. However, if a selective emitter is applied on the front to lower the $J_{oe}$ from ∼150 to ∼22 fA/cm$^2$ (by using a combination of 150 and 20 Ω/sq emitters with $AlO_x$/$SiN_x$ passivation), cell efficiency of 22.6% can be achieved with TOPCon back on a commercial Cz material. Finally, modeling shows that 23.2% efficiency can be achieved with this rear side TOPCon cell structure on Cz if screen-printed finger width can be reduced from 55 to 40 $\mu$m, and 10 Ω-cm 3 ms lifetime base material is used.

In the future work, we combine all the know-how developed in previous chapters to suggest research directions for next generation low-cost high-efficiency Si solar cell with advanced cell structures. In the following sections, first, a TOPCon cell using an epi-grown lightly doped thick field emitter is modeled to show that the use of epi can produce higher efficiency cells. Then, a process sequence for making the epi-Si TOPCon cell is proposed. Finally, the model is extended to calculate the efficiency under low-medium concentration light intensity to achieve even higher efficiency.

## *11.1 Modeling and Development of Epi-grown Emitter TOPCon Cell*

Task 5 (Section 9.2) showed that epi-grown lightly doped thick BSF ($N_s = 5 \times 10^{17}$ cm$^{-3}$, 15 $\mu$m deep) is better than the traditional diffused Al or B BSF for the p-type PERT solar cells because of reduced Auger recombination, low sheet resistance and good surface passivation. Preliminary modeling shows that the use of epi-grown

field emitter can raise the efficiency of 23.2% screen-printed TOPCon cell modeled in the previous task (Section 10.3.3 ). If the the heavily boron doped field emitter is replaced by a lightly doped and uniform epi-grown boron emitter ($5 \times 10^{17}$ cm$^{-3}$, 15 $\mu$m) with low sheet resistance of $\sim$40 $\Omega$/sq, then one can achieve better emitter passivation, reduced Auger recombination, and reduced metal shading due to low sheet resistance. An initial attempt was made in this thesis to quantify the impact of epi-grown emitter and compare it with traditional implanted/diffused emitters. Finger spacing was optimized according to the sheet resistance. The modeled LIV results for both implanted and epi-grown field emitter as function of finger spacing are shown in Figure 108. It is clear that for both cells, $V_{oc}$ and $J_{sc}$ increase as the spacing increases, but the $FF$ decreases with larger spacing. As a result, each cell has an optimum spacing for maximum efficiency. Figure 108 shows that for this epi-grown emitter design, the epi-grown TOPcon cell only gives $\sim$0.1% higher efficiency than the implant TOPCon cell mainly because of $V_{oc}$ and $FF$.

Therefore, a preliminary attempt was made to optimize the front epi-grown field emitter with different doping concentration ($10^{17}$-$5\times10^{18}$ cm$^{-3}$) and thickness (5-25 $\mu$m). The finger spacing is optimized for each emitter. The LIV results along with the emitter sheet resistance and the corresponding optimum finger spacing are shown in Figure 109. It is shown that for deep junctions (15-25 $\mu$m), low doping of $10^{17}$ cm$^{-3}$ is beneficial because of the Auger recombination. However, the best modeled efficiency of 23.4% is achieved from the 5 $\mu$m deep and $10^{18}$ cm$^{-3}$ doped uniform emitter. The modeled $V_{oc}$, $J_{sc}$ and $FF$ are 714 mV, 39.9 mA/cm$^2$, and 82.2%, respectively. It is important to recognize that 0.2% additional increase in efficiency can have appreciable impact on cost and LCOE because higher efficiency reduces material, processing, module and balance of system cost. Therefore, this area of research is highly recommended because it reduces material cost due to epi-Si substrate, cell processing cost due to built-in epi-Si junction, and module/BOS cost

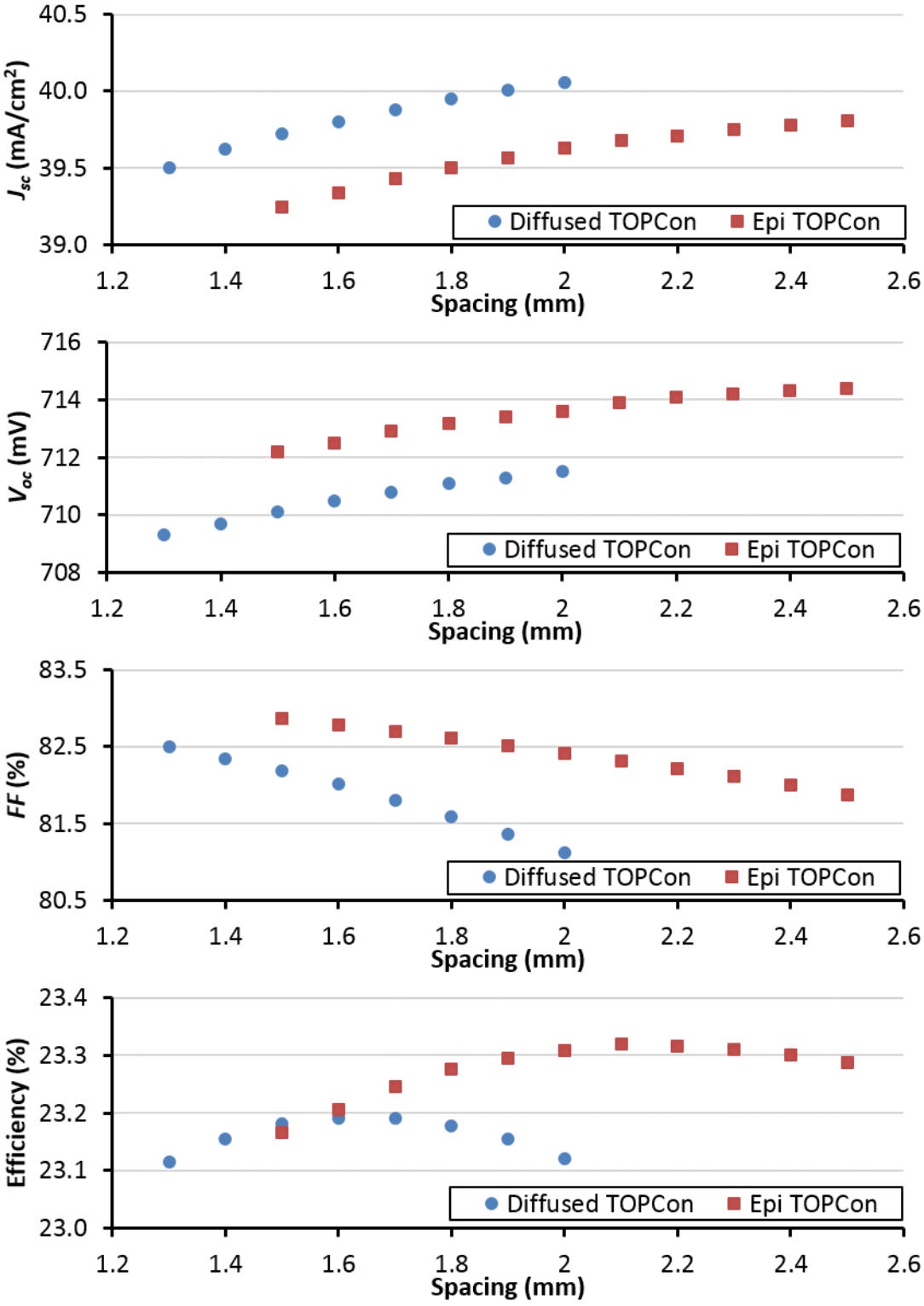



**Figure 108:** LIV as function of finger spacing and emitters.

due to higher efficiency.

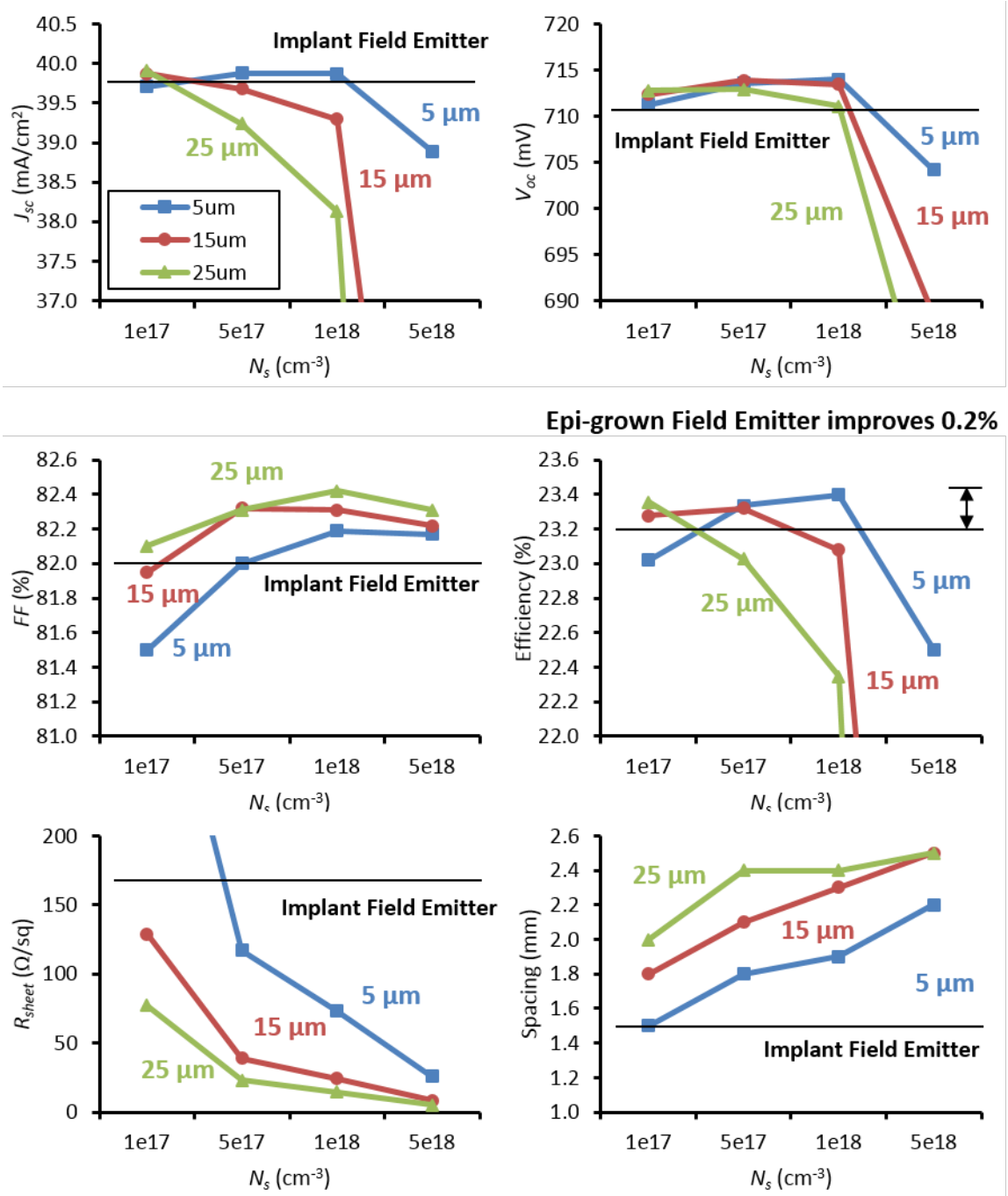



**Figure 109:** Modeled LIV data for different Epi-grown emitter TOPCon cell along with its emitter sheet resistance and optimum finger spacing.

## 11.2 *Proposed Process Flow for Epi-grown Emitter TOPCon Cell*

In addition to modeling and design of epi-Si TOPCon cells, we also propose a potential simple process sequence to make these high efficiency cells. The proposed process flow for the epi-Si TOPCon cell with built-in field emitter is shown in Figure 110. Even though the starting epi-Si substrate has a built-in lightly doped junction, a selective emitter needs to be fabricated for making ohmic contact and reduce metal recombination. Process sequence starts with a epi-grown $p^+n$ wafer structure prepared by layer

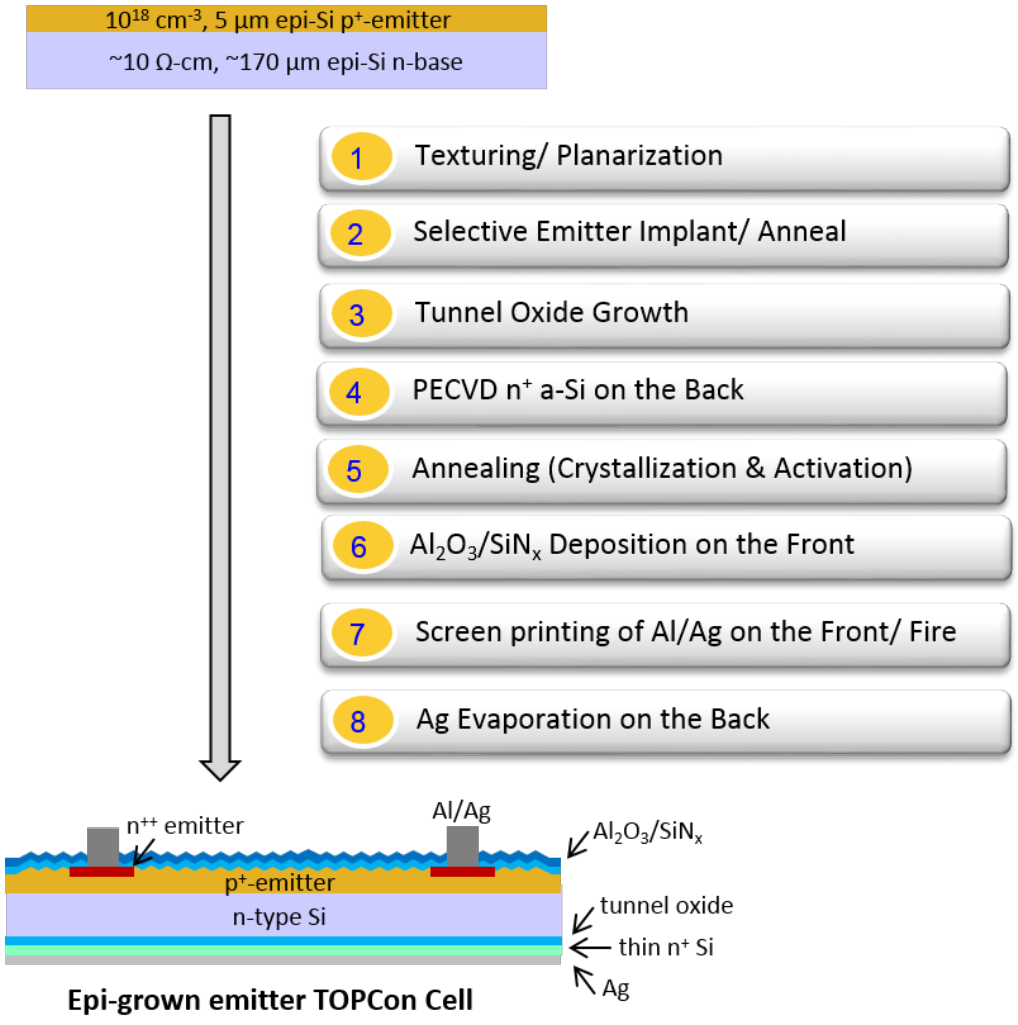



**Figure 110:** Proposed process flow for epi-grown TOPCon cell.

transfer technology as described in Task 5 (Section 9.5). The proposed cell fabrication process involves single side texturing followed by formation of selective emitter. Selective boron emitter can be formed by ion implantation and activation anneal at ∼1000 °C. After that ∼1.5 nm tunnel oxide is grown at room temperature in 68 wt% $HNO_3$ acid for 10 minutes. Phosphorus doped a-Si is then deposited by PECVD on the back and converted into P-doped Poly-Si by a 875 °C 30 minutes anneal in an inert atmosphere for crystallization and dopant activation. Then, an $AlO_x/SiN_x$ stack is deposited on the front to passivate the front boron emitter. The cell is finished by screen-printed Al/Ag on the front, contact firing, and finally Ag evaporation on the back. Note that this cell process is very similar to the one described in [127], where a 21.2% large area screen-printed TOPCon cell was achieved on commercial n-type Cz wafer. The only difference in cell processing is epi-Si substrate with built-in emitter junction and the selective emitter formation.

## *11.3 24.5% Low-medium Concentrator Si Solar Cell with Epi-grown Emitter TOPCon Cell*

Since in this thesis we also demonstrated that optimized low to medium concentrator cell design can raise the cell efficiency further, we propose applying that to epi-Si TOPCon 23.4% cells modeled in the previous section. In this section, we show preliminary modeling under low to medium concentrator and the efficiency potential of the 23.4% modeled TOPCon cell. First, the busbar shading was removed since only aperture area is considered in the concentrator cell measurement [87]. This area difference alone gives 0.6% efficiency improvement, increasing the 23.4% epi-grown TOPCon cell efficiency to 24% at one sun. As shown in Task 1 (Section 4.2.1), grid patterns were optimized to achieve higher efficiency at different concentrations. The results are shown in Figure 111 with maximum efficiency now exceeding 24.5%.

The total $R_s$ calculated for epi-grown emitter TOPCon cell with finger spacing

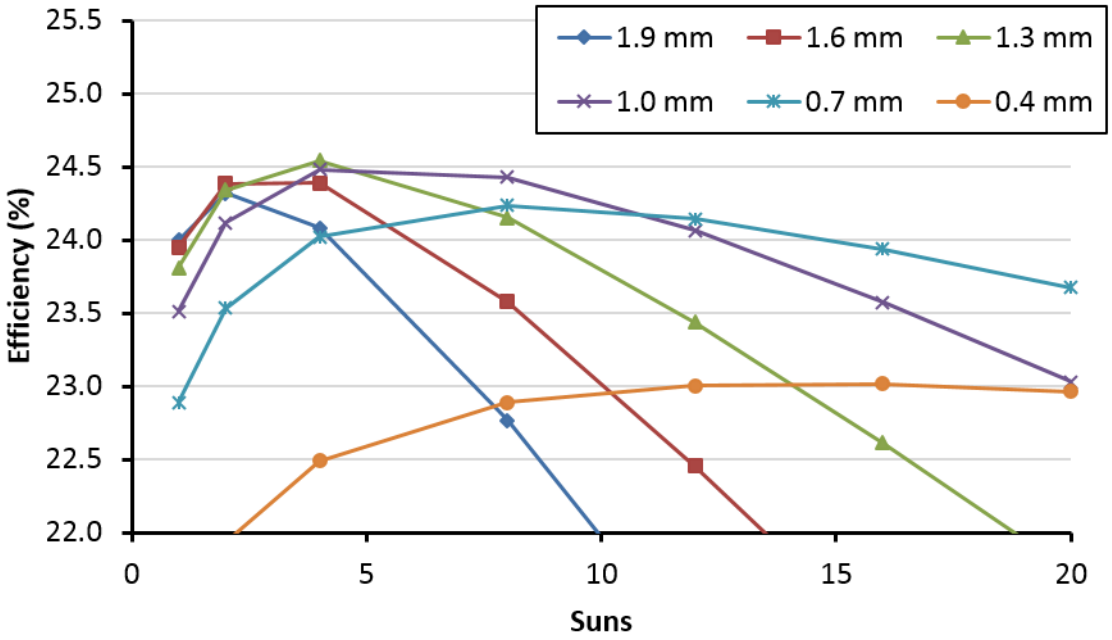



**Figure 111:** Modeled TOPCon cell efficiency under concentration with different spacing.

of 1.9, 1.6, 1.3, 1.0, 0.7, and 0.4 mm are 0.45, 0.36, 0.28, 0.23, 0.16, and 0.11 Ω-cm$^2$, respectively. Following the methodology developed in Task 1 (Section 4.2.1), we extracted the highest achievable efficiency (HAE) curve and the corresponding finger spacing from Figure 111. The result is shown in Figure 112. The highest efficiency of 24.5% at 4X is modeled with a finger spacing of 1.3 mm, which is 1.1% higher than the starting efficiency of 23.4% at one sun.

Finally a complete roadmap from 21% PERT cell today to 24.5% single side TOPCon cell is shown in Figure 113 to provide guidelines and recommendations for future research.

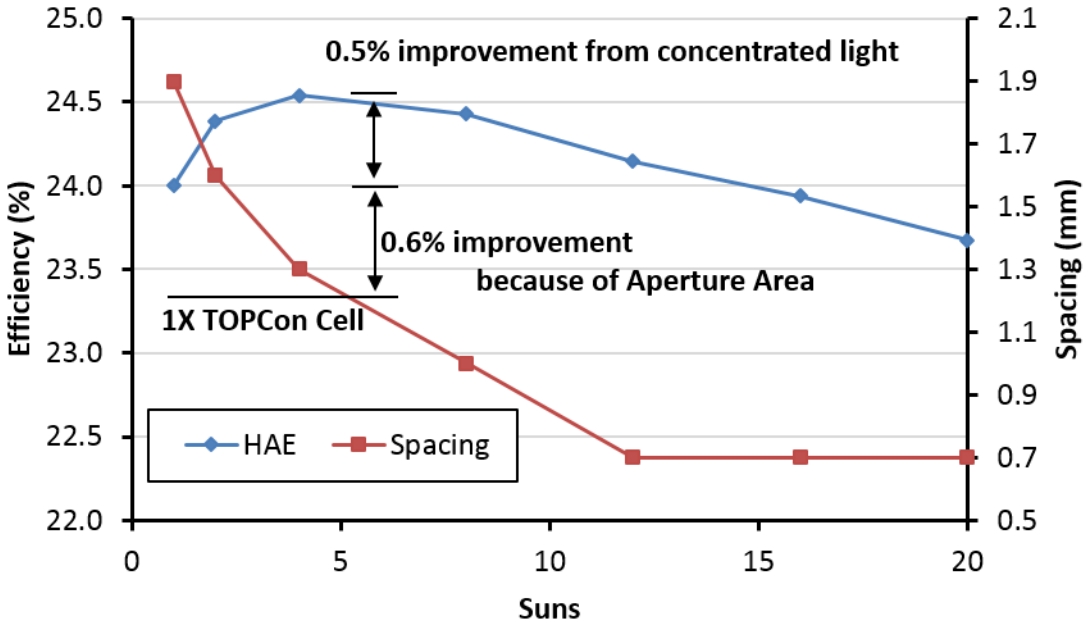



**Figure 112:** Modeled Optimum finger spacing and Highest Achievable Efficiency Curve for Epi-grown TOPCon cell.

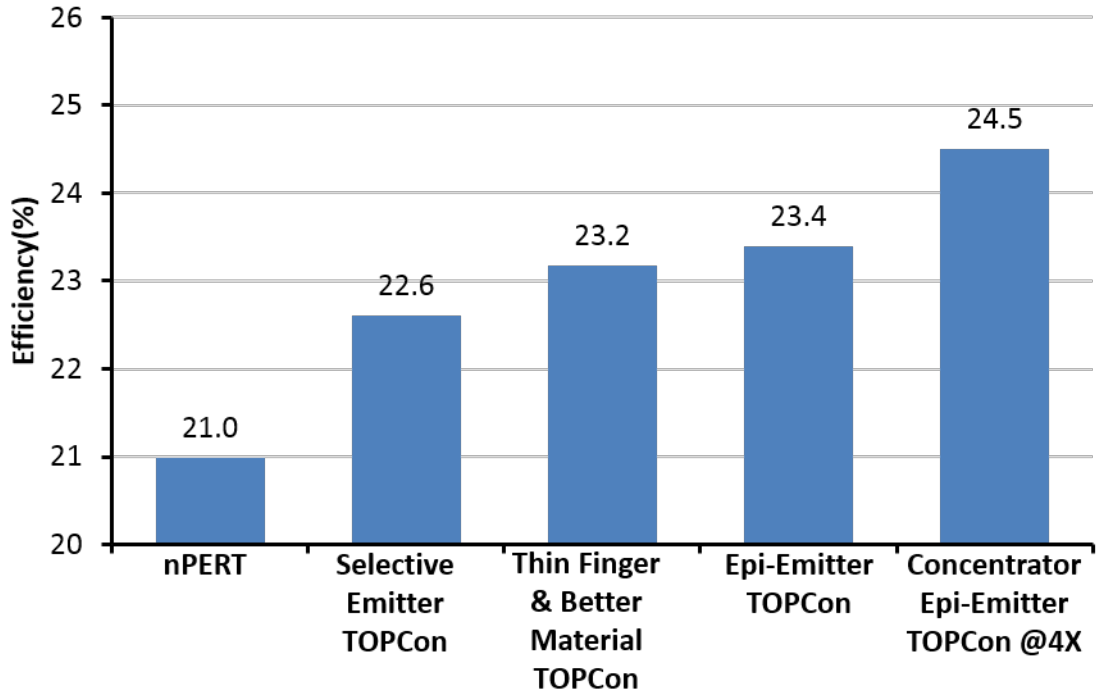



**Figure 113:** Technology roadmap from 21% n-type PERT to 24.5% concentrator Epi-grown TOPCon cell.

# APPENDIX A

# PUBLICATION FROM THE WORK

Published Journal Papers:


[1] **Chia-Wei Chen**, Yuguo Tao , Young-Woo Ok, Ajay Upadhyaya, Andrew Tam, and Ajeet Rohatgi, "Understanding and Modeling the Potential of Screen Printed Tunnel Oxide Passivated Contact Solar Cell," *Progress in Photovoltaics*, 2016 (in press).

[2] **Chia-Wei Chen**, Ruiying Hao, V. Upadhyaya, T.S. Ravi, A. Rohatgi, "Development of High Efficiency Large Area Screen Printed Solar Cells on Direct Kerfless Epitaxially Grown Mono-Crystalline Si Wafer and Structure," *Progress in Photovoltaics*, 2016 (accepted).

[3] Yuguo Tao , V. Upadhyaya, **Chia-Wei Chen**, Adam Payne, Elizabeth L Chang, Ajay Upadhyaya, Ajeet Rohatgi, "Large Area Tunnel Oxide Passivated Rear Contact n-type Si Solar Cells with 21.2% Efficiency," *Progress in Photovoltaics*, 2015 (accepted).

[4] **Chia-Wei Chen**, Ruiying Hao, V. Upadhyaya, I.B. Cooper, A. Upadhyaya, A. Zhang, T.S. Ravi, A. Rohatgi, "High-Efficiency Large-Area Screen-Printed Solar Cell on Epitaxial Thin Active Layer With Porous Si Back Reflector Using Standard Industrial Process," *IEEE Journal of Photovoltaics*, vol. 5, no. 1, Jan. 2015, pp. 123-128.

[5] **Chia-Wei Chen**, Moon Hee Kang, Vijaykumar Upadhyyaya, Aditya Kapoor, John Keith Tate, James C. Keane, Steven Ning, and Ajeet Rohatgi, "Understanding and Development of Screen-Printed Front Metallization for High-Efciency Low-to-Medium Concentrator Silicon Solar Cells," *IEEE Journal of Photovoltaics*, vol. 3, no. 3, Jul. 2013, pp. 944-951.

[6] **Chia-Wei Chen**, Abasifreke Ebong, John Renshaw, Keith Tate, Francesco Zimbardi, Ajeet Rohatgi, and Marc Finot, "Development and Understanding of High-Efciency Screen-Printed Concentrator Silicon Solar Cells," *IEEE Journal of Photovoltaics*, vol. 1, no. 2, Dec. 2011, pp. 231-235.

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Published Conference Papers:


[1] Yuguo Tao, Elizabeth Lori Chang, Ajay Upadhyaya, Brian Roundaville, Young-Woo Ok, Keeya Madani, **Chia-Wei Chen**, Keith Tate, Vijaykumar Upadhyaya, Francesco Zimbardi, Jim Keane, Adam Payne, Ajeet Rohatgi, "730 mV Implied $V_{oc}$ Enabled by Tunnel Oxide Passivated Contact with PECVD Grown and Crystallized n+ Polycrystalline Si," *42th IEEE Photovoltaic Specialists Conference*, 2015.

[2] Ruiying Hao, T.S. Ravi, V. Siva, J. Vatus, D. Miller, J. Custodio, K. Moyers, **Chia-Wei Chen**, A. Upadhyaya, A. Rohatgi, "High Efficiency Solar Cells on Direct Kerfless 156 mm Mono Crystalline Si Wafers by High Throughput Epitaxial Growth," *40th IEEE Photovoltaic Specialists Conference*, 2014, pp. 2978-2982.

[3] **Chia-Wei Chen**, Ajay Upadhyaya, Ruiying Hao, Vijaykumar Upadhyaya, Jim Keane, Francesco Zimbardi, Malka Kadish, Ivan Pham, Steven Ning, K.V. Ravi, T.S. Ravi, and Ajeet Rohatgi, "High Efficiency Screen-Printed 156cm2 Solar Cells on Thin Epitaxially Grown Silicon Material," *39th IEEE Photovoltaic Specialists Conference*, 2013, pp. 2179-2182.

[4] **Chia-Wei Chen**, Xudong Chen, Kenneth Church, Haixin Yang, Keith Tate, Ian B. Cooper, and Ajeet Rohatgi, "High Efficiency Screen Printed Low-medium Concentrator Silicon Solar Cells with Direct Printed 50 $\mu$m Wide Fingers," *38th IEEE Photovoltaic Specialists Conference*, 2012, pp.928-931.

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